NuMicro® Family

Arm® Cortex® -M0-based Microcontroller

NM1120 Series
Datasheet

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1 GENERAL DESCRIPTION

The NuMicro® NM1120 series 32-bit microcontrollers are embedded with ARM® Cortex®-M0 core for industrial applications which need high performance, high integration, and low cost. The Cortex®-M0 is the newest ARM® embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The NM1120 series can run up to 48 MHz and operate at 2.1V ~ 5.5V, -40℃ ~ 105℃, and thus can support a variety of industrial control applications which need high CPU performance. The NM1120 offers 29.5 Kbytes embedded program Flash, size configurable Data Flash (shared with program flash), 2 Kbytes Flash for the ISP, 1.5 Kbytes SPROM for security, and 4 Kbytes SRAM.

Many system level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into the NM1120 to reduce component count, board space and system cost. These useful functions make the NM1120 powerful for a wide range of applications.

Additionally, the NM1120 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

2 FEATURES

- Core
  - ARM® Cortex®-M0 core running up to 48 MHz
  - One 24-bit system timer
  - Supports low power Idle mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watch points/four breakpoints
- Built-in LDO for wide operating voltage ranged: 2.1 V to 5.5 V
- Memory
  - 29.5 Kbytes Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 2 KB Flash memory for loader (LDROM)
  - Three 0.5 KB Flash memory for security protection (SPROM)
  - 4KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
    - Switch clock sources on-the-fly
  - 4 ~ 24 MHz external crystal input (HXT)
  - 32.768 kHz external crystal input (LXT) for idle wake-up and system operation clock
  - 48 MHz internal oscillator (HIRC) (±1% accuracy at 25^0C, 5V)
    - Dynamically calibrating the HIRC OSC to 48 MHz ±1% from -40℃ to 105℃ by external 32.768K crystal oscillator (LXT)
  - 10 kHz internal low-power oscillator (LIRC) for Watchdog Timer and idle wake-up
- I/O Port
  - Up to 22 general-purpose I/O (GPIO) pins and 1 Reset pin
  - Four I/O modes:
    - Quasi-bidirectional input/output
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - Optional TTL/Schmitt trigger input
  - I/O pin can be configured as interrupt source with edge/level setting
  - Supports high driver and high sink I/O mode
  - GPIO built-in Pull-up/Pull-low resistor for selection.

- Timer
  - Provides two channel 32-bit Timers; one 8-bit pre-scalar counter with 24-bit up-timer for each timer
  - Independent clock source for each timer
  - Provides One-shot, Periodic, Toggle and Continuous operation modes
  - 24-bit up counter value is readable through TDR (Timer Data Register)
  - Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
  - Supports event counter function
  - Supports Toggle Output mode
  - Supports wake-up from Idle or Power-down mode
- Continuous Capture
  - Timer0, Timer1 and Systick have support Continuous Capture function which can Continuous Capture at most 4 edges on one signal
- Enhanced Input Capture
  - One units of 24-bit input capture counter
  - Capture surce:
    - I/O inputs: ECAP0, ECAP1 and ECAP2
    - ACMP Trigger
    - ADC Trigger
- WDT (Watchdog Timer)
  - Programmable clock source and time-out period
  - Supports wake-up function in Power-down mode and Idle mode
  - Interrupt or reset selectable on watchdog time-out
- EPWM(Enhanced PWM Generator)
  - Supports a built-in 16-bit PWM clock generators, providing six PWM outputs or three complementary paired PWM outputs
  - Shared same as clock source, clock divider, period and dead-zone generator
  - Supports group/independent/ complementary modes
  - Supports One-shot or Auto-reload mode
  - Supports Edge-aligned and Center-aligned type
  - Supports Asymmetric mode
  - Programmable dead-zone insertion between complementary channels
  - Each output has independent polarity setting control
  - Hardware fault brake and software brake protections
  - Supports rising, falling, central, period, and fault break interrupts
  - Supports duty/period trigger A/D conversion
  - Timer comparing matching event trigger PWM to do phase change
  - Supports comparator event trigger PWM to force PWM output low for current period

- Provides interrupt accumulation function

- BPWM (Basic PWM Generator)
  - One 16-bit PWM generator which supports one 8-bit pre-scalar, one clock divider, two PWM timers (down counter) and one dead-zone generator
  - Two independent outputs or one complementary paired outputs.
  - PWM Interrupt request synchronized with PWM period
  - Edge-aligned type or Center-aligned type option
- USCI (Universal Serial Control Interface Controller)
  - Two USCI devices
  - Supports to be configured as UART, SPI or I²C individually
  - Supports programmable baud-rate generator
- ADC (Analog-to-Digital Converter)
  - 12-bit ADC with 1M SPS
  - Supports 2 sample/hold
  - Up to 8-ch single-end input from I/O and one internal input from band-gap.
  - Conversion started either by software trigger, PWM trigger, ACMP trigger or external pin trigger
  - Supports temperature sensor for measurement chip temperature
  - Supports Simultaneous and Sequential function to continuous conversion 4 channels maximum.
- Programmable Gain Amplifier (PGA)
  - Supports 8 level gain selects from 1, 2, 3, 5, 7, 9, 11 and 13.
  - Unity gain frequency up to 8MHz
- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Built-in CRV (comparator reference voltage)
  - Supports Hysteresis function
  - Interrupt when compared results changed
- Hardware Divider
  - Signed (two's complement) integer calculation
  - 32-bit dividend with 16-bit divisor calculation capacity
  - 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
  - Divided by zero warning flag
  - 6 HCLK clocks taken for one cycle calculation
  - Waiting for calculation ready automatically when reading quotient and remainder
- ISP (In-System Programming) and ICP (In-Circuit Programming)

- BOD (Brown-out Detector)
  - 8 programmable threshold levels: 4.3V/4.0V/3.7V/3.0V/2.7V/2.4V/2.2V/2.0V
  - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
- Operating Temperature: -40℃~105℃
- Reliability: EFT > ± 4KV, ESD HBM pass 4KV
- Packages:
  - 28-pin TSSOP, 20-pin TSSOP, 20-pin QFN
  - Package is Halogen-free, RoHS-compliant and TSCA-compliant.

3 ABBREVIATIONS

3.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
BOD	Brown-out Detection
DAP	Debug Access Port
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	48 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
ICP	In Circuit Programming
ISP	In System Programming
ISR	Interrupt Service Routine
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LXT	32.768 kHz External Low Speed Crystal Oscillator
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer

Table 3.1-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 Selection Guide

4.1.1 NuMicro® NM1120 Series Selection Guide

Part Number (Order Number)	Flash (KB)	SRAM (KB)	ISP Loader ROM (KB)	Data Flash	I/O	Timer	Connectivity			IRC 48 MHz*	BOD	PWM	Analog Comp.	PGA	ADC (12-bit)	Temperature Sensor	ICP/ISPI/AP	Package
							USCI											
							UART*	I²C	SPI									
NM1120FC1AE	29.5	4	2	√	18	2	2	2	2	1	1	6	2	1	8x12bit	1	√	TSSOP20
NM1120EC1AE	29.5	4	2	√	22	2	2	2	2	1	1	6	2	1	8x12bit	1	√	TSSOP28
NM1120XC1AE	29.5	4	2	√	18	2	2	2	2	1	1	6	2	1	8x12bit	1	√	QFN20

Table 4.1-1 NuMicro® NM1120 Base Series Selection Guide

4.2 Pin Configuration

4.2.1 NuMicro® NM1120 Series TSSOP28 Pin Diagram

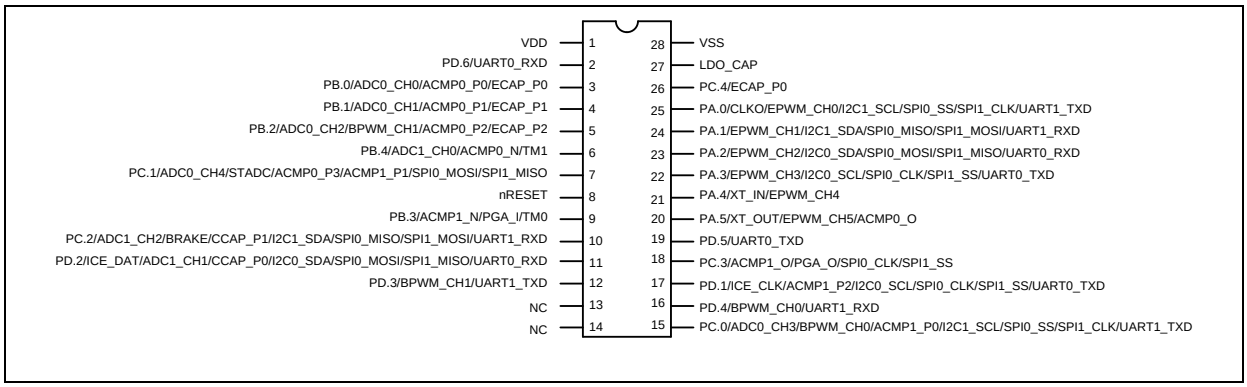


Figure 4.2-1 NuMicro® NM1120 Base Series TSSOP 28-pin Diagram

4.2.2 NuMicro® NM1120 Series TSSOP20 Pin Diagram

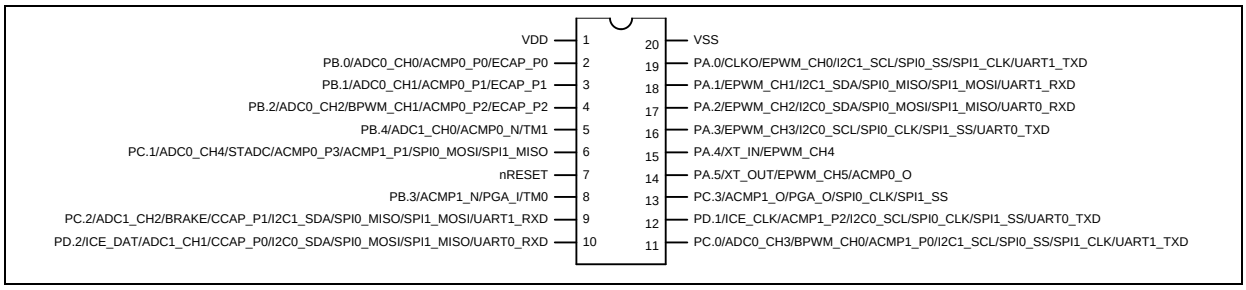


Figure 4.2-2 NuMicro® NM1120 Base Series TSSOP 20-pin Diagram

4.2.3 NuMicro® NM1120 Series QFN20 Pin Diagram

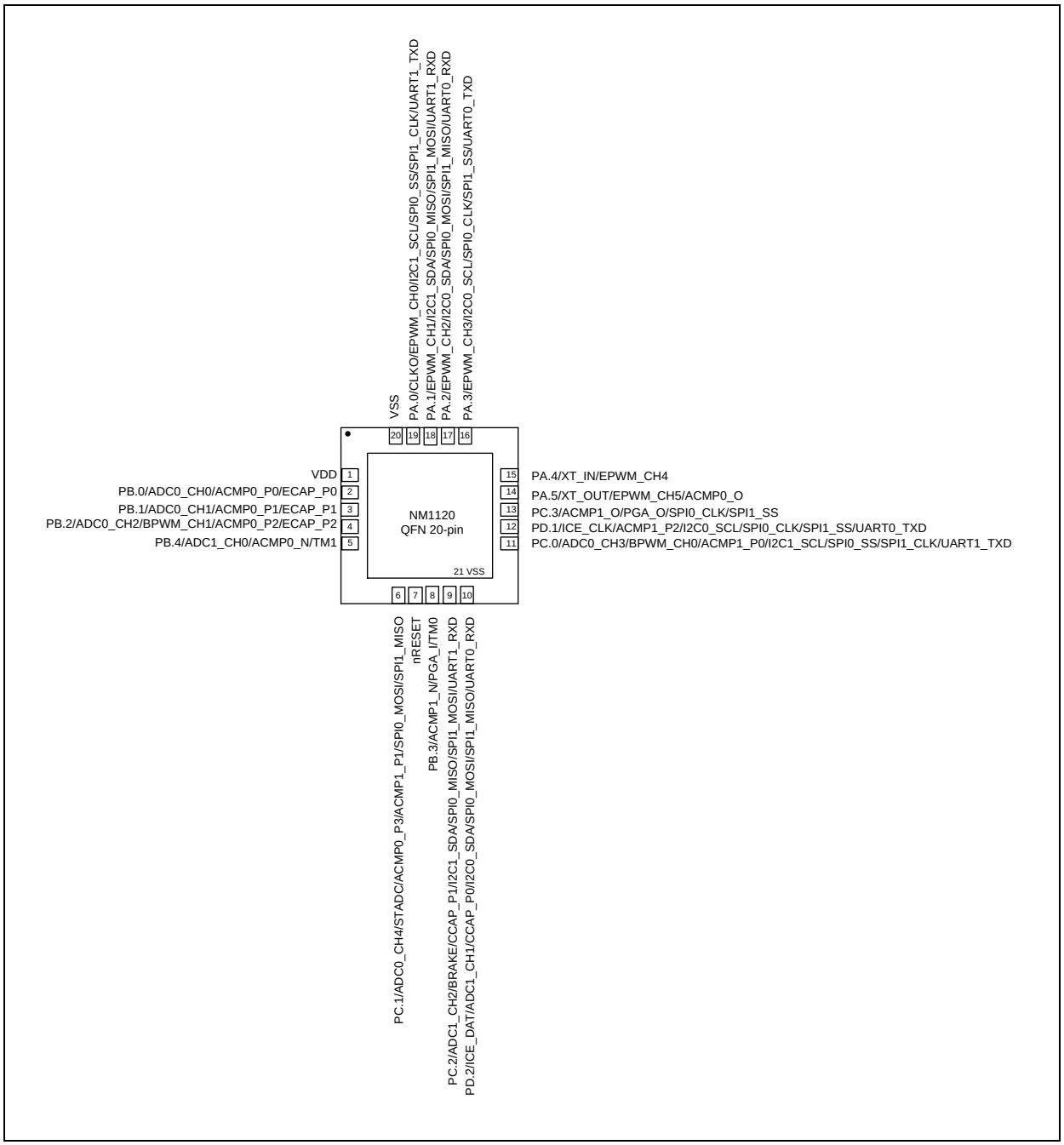


Figure 4.2-3 NuMicro® NM1120 Base Series QFN 20-pin Diagram

4.3 Pin Description

4.3.1 NM1120 Series Pin Description Overview

	Alternative function , MFP_0 means setting MFP[3:0]=0x0, MFP_5 means MFP[3:0]=0x5																													
GPIO	ICE XTAL		ADC		PWM_BRAKE		ACMP0		ACMP1		PGA(OP)		TIMER		I2C		SPIO		SPI1		UART		
MFP_0	MFP_1		MFP_2		MFP_3		MFP_4		MFP_5		MFP_6		MFP_7		MFP_8		MFP_9		MFP_A		MFP_B		MFP_C
GPA0	CLKO	O			EPWM_CH0	O									I²C1_SCL	I/O	SPI0_SS	I/O	SPI1_CLK	I/O	UART1_TXD	O	
GPA1					EPWM_CH1	O									I²C1_SDA	I/O	SPI0_MISO	I/O	SPI1_MOSI	I/O	UART1_RXD	I	
GPA2					EPWM_CH2	O									I²C0_SDA	I/O	SPI0_MOSI	I/O	SPI1_MISO	I/O	UART0_RXD	I	
GPA3					EPWM_CH3	O									I²C0_SCL	I/O	SPI0_CLK	I/O	SPI1_SS	I/O	UART0_TXD	O	
GPA4	XT_IN	A			EPWM_CH4	O																	
GPA5	XT_OUT	A			EPWM_CH5	O	ACMP0_O	O															
GPB0			ADC0_CH0	A			ACMP0_P0	A					ECAP0	I									
GPB1			ADC0_CH1	A			ACMP0_P1	A					ECAP1	I									
GPB2			ADC0_CH2	A	BPWM_CH1	O	ACMP0_P2	A					ECAP2	I									
GPB3									ACMP1_N	A	PGA_I	A	T0	I/O									
GPB4			ADC1_CH0	A			ACMP0_N	A					T1	I/O									
GPC0			ADC0_CH3	A	BPWM_CH0	O			ACMP1_P0	A					I²C1_SCL	I/O	SPI0_SS	I/O	SPI1_CLK	I/O	UART1_TXD	O	
GPC1			ADC0_CH4	A	STADC	I	ACMP0_P3	A	ACMP1_P1	A							SPI0_MOSI	I/O	SPI1_MISO	I/O			
GPC2			ADC1_CH2	A	PWM_BRAKE	I							CCAP	I	I²C1_SDA	I/O	SPI0_MISO	I/O	SPI1_MOSI	I/O	UART1_RXD	I	
GPC3									ACMP1_O	O	PGA_O	A					SPI0_CLK	I/O	SPI1_SS	I/O			
GPC4													ECAP0	I									
nRESET																							
GPD1	ICE_CLK	I							ACMP1_P2	A					I²C0_SCL	I/O	SPI0_CLK	I/O	SPI1_SS	I/O	UART0_TXD	O	
GPD2	ICE_DAT	I/O	ADC1_CH1	A									CCAP	I	I²C0_SDA	I/O	SPI0_MOSI	I/O	SPI1_MISO	I/O	UART0_RXD	I	
GPD3					BPWM_CH1	O															UART1_TXD	O	
GPD4					BPWM_CH0	O															UART1_RXD	I	
GPD5																					UART0_TXD	O	
GPD6																					UART0_RXD	I	
VDD																							
VSS																							

4.3.2 NM1120 Series Pin Description

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFP)

PA.0 MFP0 means SYS_GPA_MFP[3:0]=0x0.

PA.4 MFP5 means SYS_GPA_MFP[19:16]=0x5.

MFP only configures the ouput data or input data of PAD, the direction of PAD were configured by PMD.

The priority of MFP in the same multi-function was GPA > GPB > GPC > GPD.

The type A of multi-function needs to be configured to be input port.

4.3.2.1 NM1120 Series TSSOP28 Pin Description

Pin No.	Pin Name	Type	MFP*	Description
1	VDD	A	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital function.
2	PD.6	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MFPB	Data receiver input pin for UART0.
3	PB.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH0	A	MFP2	ADC0 channel0 analog input.
	ACMP0_P0	A	MFP4	Analog comparator0 positive input pin.
	ECAP_P0	I	MFP7	Enhanced Input Capture input pin
4	PB.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH1	A	MFP2	ADC0 channel1 analog input.
	ACMP0_P1	A	MFP4	Analog comparator0 positive input pin.
	ECAP_P1	I	MFP7	Enhanced Input Capture input pin
5	PB.2	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH2	A	MFP2	ADC0 channel2 analog input.
	BPWM_CH1	I/O	MFP3	PWM channel1 output/capture input.
	ACMP0_P2	A	MFP4	Analog comparator0 positive input pin.
	ECAP_P2	I	MFP7	Enhanced Input Capture input pin
6	PB.4	I/O	MFP0	General purpose digital I/O pin.
	ADC1_CH0	A	MFP2	ADC1 channel0 analog input.
	ACMP0_N	A	MFP4	Analog comparator0 negative input pin.
	TM1	I/O	MFP7	Timer1 event counter input / toggle output
7	PC.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH4	A	MFP2	ADC0 channel4 analog input.
	STADC	I	MFP3	ADC external trigger input.

Pin No.	Pin Name	Type	MFP*	Description
	ACMP0_P3	A	MFP4	Analog comparator0 positive input pin.
	ACMP1_P1	A	MFP5	Analog comparator1 positive input pin.
	SPI0_MOSI	I/O	MFP9	SPI0 1st MOSI (Master Out, Slave In) pin.
	SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
8	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
9	PB.3	I/O	MFP0	General purpose digital I/O pin.
	ACMP1_N	A	MFP5	Analog comparator1 negative input pin.
	PGA_I	A	MFP6	PGA input pin
	TM0	I/O	MFP7	Timer0event counter input / toggle output
10	PC.2	I/O	MFP0	General purpose digital I/O pin.
	ADC1_CH2	A	MFP2	ADC1 channel2 analog input.
	BRAKE	I	MFP3	Brake input pin of EPWM.
	CCAP_P1	I	MFP7	Timer Continuous Capture input pin
	I2C1_SDA	I/O	MFP8	I^2C1 data input/output pin.
	SPI0_MISO	I/O	MFP9	SPI0 1st MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	MFPA	SPI1 MOSI (Master Out, Slave In) pin.
	UART1_RXD	I	MFPB	Data receiver input pin for UART1.
11	PD.2	I/O	MFP0	General purpose digital I/O pin.
	ICE_DAT	I/O	MFP1	Serial wired debugger data pin
	ADC1_CH1	A	MFP2	ADC1 channel1 analog input.
	CCAP_P0	I	MFP7	Timer Continuous Capture input pin
	I2C0_SDA	I/O	MFP8	I^2C0 data input/output pin.
	SPI0_MOSI	I/O	MFP9	SPI0 1st MOSI (Master Out, Slave In) pin.
	SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
	UART0_RXD	I	MFPB	Data receiver input pin for UART0.
12	PD.3	I/O	MFP0	General purpose digital I/O pin.
	BPWM_CH1	I/O	MFP3	PWM channel1 output/capture input.
	UART1_TXD	O	MFPB	Data transmitter output pin for UART1.
13	NC			No Connection
14	NC			No Connection
15	PC.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH3	A	MFP2	ADC0 channel3 analog input.

Pin No.	Pin Name	Type	MFP*	Description
	BPWM_CH0	I/O	MFP3	PWM channel0 output/capture input.
	ACMP1_P0	A	MFP5	Analog comparator1 positive input pin.
	I2C1_SCL	I/O	MFP8	I^2C1 clock pin.
	SPI0_SS	I/O	MFP9	SPI0 slave select pin.
	SPI1_CLK	I/O	MFPA	SPI1 serial clock pin
	UART1_TXD	O	MFPB	Data transmitter output pin for UART1.
16	PD.4	I/O	MFP0	General purpose digital I/O pin.
	BPWM_CH0	I/O	MFP3	PWM channel0 output/capture input.
	UART1_RXD	I	MFPB	Data receiver input pin for UART1.
17	PD.1	I/O	MFP0	General purpose digital I/O pin.
	ICE_CLK	I	MFP1	Serial wired debugger clock pin
	ACMP1_P2	A	MFP5	Analog comparator1 positive input pin.
	I2C0_SCL	I/O	MFP8	I^2C0 clock pin.
	SPI0_CLK	I/O	MFP9	SPI0 serial clock pin.
	SPI1_SS	I/O	MFPA	SPI1 slave select pin
	UART0_TXD	O	MFPB	Data transmitter output pin for UART0.
18	PC.3	I/O	MFP0	General purpose digital I/O pin.
	ACMP1_O	O	MFP5	Analog comparator1 output.
	PGA_O	A	MFP6	PGA output pin
	SPI0_CLK	I/O	MFP9	SPI0 serial clock pin.
	SPI1_SS	I/O	MFPA	SPI1 slave select pin
19	PD.5	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MFPB	Data transmitter output pin for UART0.
20	PA.5	I/O	MFP0	General purpose digital I/O pin.
	XT_OUT	O	MFP1	External 4~24 MHz (high speed) crystal output pin.
	EPWM_CH5	I/O	MFP3	PWM channel5 output/capture input.
	ACMP0_O	O	MFP4	Analog comparator0 output.
21	PA.4	I/O	MFP0	General purpose digital I/O pin.
	XT_IN	I	MFP1	External 4~24 MHz (high speed) crystal input pin.
	EPWM_CH4	I/O	MFP3	PWM channel4 output/capture input.
22	PA.3	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH3	I/O	MFP3	PWM channel3 output/capture input.
	I2C0_SCL	I/O	MFP8	I^2C0 clock pin.

Pin No.	Pin Name	Type	MFP*	Description
	SPI0_CLK	I/O	MFP9	SPI0 serial clock pin.
	SPI1_SS	I/O	MFPA	SPI1 slave select pin
	UART0_TXD	O	MFPB	Data transmitter output pin for UART0.
23	PA.2	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH2	I/O	MFP3	PWM channel2 output/capture input.
	I2C0_SDA	I/O	MFP8	I^2C0 data input/output pin.
	SPI0_MOSI	I/O	MFP9	SPI0 1st MOSI (Master Out, Slave In) pin.
	SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
	UART0_RXD	I	MFPB	Data receiver input pin for UART0.
24	PA.1	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH1	I/O	MFP3	PWM channel1 output/capture input.
	I2C1_SDA	I/O	MFP8	I^2C1 data input/output pin.
	SPI0_MISO	I/O	MFP9	SPI0 1st MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	MFPA	SPI1 MOSI (Master Out, Slave In) pin.
	UART1_RXD	I	MFPB	Data receiver input pin for UART1.
25	PA.0	I/O	MFP0	General purpose digital I/O pin.
	CLKO	O	MFP1	Clock Out
	EPWM_CH0	I/O	MFP3	PWM channel0 output/capture input.
	I2C1_SCL	I/O	MFP8	I^2C1 clock pin.
	SPI0_SS	I/O	MFP9	SPI0 slave select pin.
	SPI1_CLK	I/O	MFPA	SPI1 serial clock pin
	UART1_TXD	O	MFPB	Data transmitter output pin for UART1.
26	PC.4	I/O	MFP0	General purpose digital I/O pin.
	ECAP_P0	I	MFP7	Enhanced Input Capture input pin
27	LDO_CAP	A	MFP0	LDO output pin. **Note:** Recommend to connect a 1uF CAP to the pin.
28	V_{SS}	A	MFP0	Ground pin for digital circuit.

Table 4.3-1 TSSOP28 Pin Description

4.3.2.2 NM1120 Series TSSOP20 Pin Description

Pin No.	Pin Name	Type	MFP*	Description
1	VDD	A	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital function.
2	PB.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH0	A	MFP2	ADC0 channel0 analog input.
	ACMP0_P0	A	MFP4	Analog comparator0 positive input pin.
	ECAP_P0	I	MFP7	Enhanced Input Capture input pin
3	PB.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH1	A	MFP2	ADC0 channel1 analog input.
	ACMP0_P1	A	MFP4	Analog comparator0 positive input pin.
	ECAP_P1	I	MFP7	Enhanced Input Capture input pin
4	PB.2	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH2	A	MFP2	ADC0 channel2 analog input.
	BPWM_CH1	I/O	MFP3	PWM channel1 output/capture input.
	ACMP0_P2	A	MFP4	Analog comparator0 positive input pin.
	ECAP_P2	I	MFP7	Enhanced Input Capture input pin
5	PB.4	I/O	MFP0	General purpose digital I/O pin.
	ADC1_CH0	A	MFP2	ADC1 channel0 analog input.
	ACMP0_N	A	MFP4	Analog comparator0 negative input pin.
	TM1	I/O	MFP7	Timer1 event counter input / toggle output
6	PC.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH4	A	MFP2	ADC0 channel4 analog input.
	STADC	I	MFP3	ADC external trigger input.
	ACMP0_P3	A	MFP4	Analog comparator0 positive input pin.
	ACMP1_P1	A	MFP5	Analog comparator1 positive input pin.
	SPI0_MOSI	I/O	MFP9	SPI0 1st MOSI (Master Out, Slave In) pin.
	SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
7	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
8	PB.3	I/O	MFP0	General purpose digital I/O pin.
	ACMP1_N	A	MFP5	Analog comparator1 negative input pin.
	PGA_I	A	MFP6	PGA input pin
	TM0	I/O	MFP7	Timer0event counter input / toggle output

Pin No.	Pin Name	Type	MFP*	Description
9	PC.2	I/O	MFP0	General purpose digital I/O pin.
	ADC1_CH2	A	MFP2	ADC1 channel2 analog input.
	BRAKE	I	MFP3	Brake input pin of EPWM.
	CCAP_P1	I	MFP7	Timer Continuous Capture input pin
	I2C1_SDA	I/O	MFP8	I^2C1 data input/output pin.
	SPI0_MISO	I/O	MFP9	SPI0 1st MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	MFPA	SPI1 MOSI (Master Out, Slave In) pin.
	UART1_RXD	I	MFPB	Data receiver input pin for UART1.
10	PD.2	I/O	MFP0	General purpose digital I/O pin.
	ICE_DAT	I/O	MFP1	Serial wired debugger data pin
	ADC1_CH1	A	MFP2	ADC1 channel1 analog input.
	CCAP_P0	I	MFP7	Timer Continuous Capture input pin
	I2C0_SDA	I/O	MFP8	I^2C0 data input/output pin.
	SPI0_MOSI	I/O	MFP9	SPI0 1st MOSI (Master Out, Slave In) pin.
	SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
	UART0_RXD	I	MFPB	Data receiver input pin for UART0.
11	PC.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH3	A	MFP2	ADC0 channel3 analog input.
	BPWM_CH0	I/O	MFP3	PWM channel0 output/capture input.
	ACMP1_P0	A	MFP5	Analog comparator1 positive input pin.
	I2C1_SCL	I/O	MFP8	I^2C1 clock pin.
	SPI0_SS	I/O	MFP9	SPI0 slave select pin.
	SPI1_CLK	I/O	MFPA	SPI1 serial clock pin
	UART1_TXD	O	MFPB	Data transmitter output pin for UART1.
12	PD.1	I/O	MFP0	General purpose digital I/O pin.
	ICE_CLK	I	MFP1	Serial wired debugger clock pin
	ACMP1_P2	A	MFP5	Analog comparator1 positive input pin.
	I2C0_SCL	I/O	MFP8	I^2C0 clock pin.
	SPI0_CLK	I/O	MFP9	SPI0 serial clock pin.
	SPI1_SS	I/O	MFPA	SPI1 slave select pin
	UART0_TXD	O	MFPB	Data transmitter output pin for UART0.
13	PC.3	I/O	MFP0	General purpose digital I/O pin.
	ACMP1_O	O	MFP5	Analog comparator1 output.

Pin No.	Pin Name	Type	MFP*	Description
	PGA_O	A	MFP6	PGA output pin
	SPI0_CLK	I/O	MFP9	SPI0 serial clock pin.
	SPI1_SS	I/O	MFPA	SPI1 slave select pin
14	PA.5	I/O	MFP0	General purpose digital I/O pin.
	XT_OUT	O	MFP1	External 4~24 MHz (high speed) crystal output pin.
	EPWM_CH5	I/O	MFP3	PWM channel5 output/capture input.
	ACMP0_O	O	MFP4	Analog comparator0 output.
15	PA.4	I/O	MFP0	General purpose digital I/O pin.
	XT_IN	I	MFP1	External 4~24 MHz (high speed) crystal input pin.
	EPWM_CH4	I/O	MFP3	PWM channel4 output/capture input.
16	PA.3	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH3	I/O	MFP3	PWM channel3 output/capture input.
	I2C0_SCL	I/O	MFP8	I^2C0 clock pin.
	SPI0_CLK	I/O	MFP9	SPI0 serial clock pin.
	SPI1_SS	I/O	MFPA	SPI1 slave select pin
	UART0_TXD	O	MFPB	Data transmitter output pin for UART0.
17	PA.2	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH2	I/O	MFP3	PWM channel2 output/capture input.
	I2C0_SDA	I/O	MFP8	I^2C0 data input/output pin.
	SPI0_MOSI	I/O	MFP9	SPI0 1st MOSI (Master Out, Slave In) pin.
	SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
	UART0_RXD	I	MFPB	Data receiver input pin for UART0.
18	PA.1	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH1	I/O	MFP3	PWM channel1 output/capture input.
	I2C1_SDA	I/O	MFP8	I^2C1 data input/output pin.
	SPI0_MISO	I/O	MFP9	SPI0 1st MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	MFPA	SPI1 MOSI (Master Out, Slave In) pin.
	UART1_RXD	I	MFPB	Data receiver input pin for UART1.
19	PA.0	I/O	MFP0	General purpose digital I/O pin.
	CLKO	O	MFP1	Clock Out
	EPWM_CH0	I/O	MFP3	PWM channel0 output/capture input.
	I2C1_SCL	I/O	MFP8	I^2C1 clock pin.
	SPI0_SS	I/O	MFP9	SPI0 slave select pin.

Pin No.	Pin Name	Type	MFP*	Description
	SPI1_CLK	I/O	MFPA	SPI1 serial clock pin
	UART1_TXD	O	MFPB	Data transmitter output pin for UART1.
20	V_{SS}	A	MFP0	Ground pin for digital circuit.

Table 4.3-2 TSSOP20 Pin Description

4.3.2.3 NM1120 Series QFN20 Pin Description

Pin No.	Pin Name	Type	MFP*	Description
1	VDD	A	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital function.
2	PB.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH0	A	MFP2	ADC0 channel0 analog input.
	ACMP0_P0	A	MFP4	Analog comparator0 positive input pin.
	ECAP_P0	I	MFP7	Enhanced Input Capture input pin
3	PB.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH1	A	MFP2	ADC0 channel1 analog input.
	ACMP0_P1	A	MFP4	Analog comparator0 positive input pin.
	ECAP_P1	I	MFP7	Enhanced Input Capture input pin
4	PB.2	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH2	A	MFP2	ADC0 channel2 analog input.
	BPWM_CH1	I/O	MFP3	PWM channel1 output/capture input.
	ACMP0_P2	A	MFP4	Analog comparator0 positive input pin.
	ECAP_P2	I	MFP7	Enhanced Input Capture input pin
5	PB.4	I/O	MFP0	General purpose digital I/O pin.
	ADC1_CH0	A	MFP2	ADC1 channel0 analog input.
	ACMP0_N	A	MFP4	Analog comparator0 negative input pin.
	TM1	I/O	MFP7	Timer1 event counter input / toggle output
6	PC.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH4	A	MFP2	ADC0 channel4 analog input.
	STADC	I	MFP3	ADC external trigger input.
	ACMP0_P3	A	MFP4	Analog comparator0 positive input pin.
	ACMP1_P1	A	MFP5	Analog comparator1 positive input pin.
	SPI0_MOSI	I/O	MFP9	SPI0 1st MOSI (Master Out, Slave In) pin.
	SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
7	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
8	PB.3	I/O	MFP0	General purpose digital I/O pin.
	ACMP1_N	A	MFP5	Analog comparator1 negative input pin.
	PGA_I	A	MFP6	PGA input pin
	TM0	I/O	MFP7	Timer0event counter input / toggle output

Pin No.	Pin Name	Type	MFP*	Description
9	PC.2	I/O	MFP0	General purpose digital I/O pin.
	ADC1_CH2	A	MFP2	ADC1 channel2 analog input.
	BRAKE	I	MFP3	Brake input pin of EPWM.
	CCAP_P1	I	MFP7	Timer Continuous Capture input pin
	I2C1_SDA	I/O	MFP8	I^2C1 data input/output pin.
	SPI0_MISO	I/O	MFP9	SPI0 1st MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	MFPA	SPI1 MOSI (Master Out, Slave In) pin.
	UART1_RXD	I	MFPB	Data receiver input pin for UART1.
10	PD.2	I/O	MFP0	General purpose digital I/O pin.
	ICE_DAT	I/O	MFP1	Serial wired debugger data pin
	ADC1_CH1	A	MFP2	ADC1 channel1 analog input.
	CCAP_P0	I	MFP7	Timer Continuous Capture input pin
	I2C0_SDA	I/O	MFP8	I^2C0 data input/output pin.
	SPI0_MOSI	I/O	MFP9	SPI0 1st MOSI (Master Out, Slave In) pin.
	SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
	UART0_RXD	I	MFPB	Data receiver input pin for UART0.
11	PC.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH3	A	MFP2	ADC0 channel3 analog input.
	BPWM_CH0	I/O	MFP3	PWM channel0 output/capture input.
	ACMP1_P0	A	MFP5	Analog comparator1 positive input pin.
	I2C1_SCL	I/O	MFP8	I^2C1 clock pin.
	SPI0_SS	I/O	MFP9	SPI0 slave select pin.
	SPI1_CLK	I/O	MFPA	SPI1 serial clock pin
	UART1_TXD	O	MFPB	Data transmitter output pin for UART1.
12	PD.1	I/O	MFP0	General purpose digital I/O pin.
	ICE_CLK	I	MFP1	Serial wired debugger clock pin
	ACMP1_P2	A	MFP5	Analog comparator1 positive input pin.
	I2C0_SCL	I/O	MFP8	I^2C0 clock pin.
	SPI0_CLK	I/O	MFP9	SPI0 serial clock pin.
	SPI1_SS	I/O	MFPA	SPI1 slave select pin
	UART0_TXD	O	MFPB	Data transmitter output pin for UART0.
13	PC.3	I/O	MFP0	General purpose digital I/O pin.
	ACMP1_O	O	MFP5	Analog comparator1 output.

Pin No.	Pin Name	Type	MFP*	Description
	PGA_O	A	MFP6	PGA output pin
	SPI0_CLK	I/O	MFP9	SPI0 serial clock pin.
	SPI1_SS	I/O	MFPA	SPI1 slave select pin
14	PA.5	I/O	MFP0	General purpose digital I/O pin.
	XT_OUT	O	MFP1	External 4~24 MHz (high speed) crystal output pin.
	EPWM_CH5	I/O	MFP3	PWM channel5 output/capture input.
	ACMP0_O	O	MFP4	Analog comparator0 output.
15	PA.4	I/O	MFP0	General purpose digital I/O pin.
	XT_IN	I	MFP1	External 4~24 MHz (high speed) crystal input pin.
	EPWM_CH4	I/O	MFP3	PWM channel4 output/capture input.
16	PA.3	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH3	I/O	MFP3	PWM channel3 output/capture input.
	I2C0_SCL	I/O	MFP8	I^2C0 clock pin.
	SPI0_CLK	I/O	MFP9	SPI0 serial clock pin.
	SPI1_SS	I/O	MFPA	SPI1 slave select pin
	UART0_TXD	O	MFPB	Data transmitter output pin for UART0.
17	PA.2	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH2	I/O	MFP3	PWM channel2 output/capture input.
	I2C0_SDA	I/O	MFP8	I^2C0 data input/output pin.
	SPI0_MOSI	I/O	MFP9	SPI0 1st MOSI (Master Out, Slave In) pin.
	SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
	UART0_RXD	I	MFPB	Data receiver input pin for UART0.
18	PA.1	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH1	I/O	MFP3	PWM channel1 output/capture input.
	I2C1_SDA	I/O	MFP8	I^2C1 data input/output pin.
	SPI0_MISO	I/O	MFP9	SPI0 1st MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	MFPA	SPI1 MOSI (Master Out, Slave In) pin.
	UART1_RXD	I	MFPB	Data receiver input pin for UART1.
19	PA.0	I/O	MFP0	General purpose digital I/O pin.
	CLKO	O	MFP1	Clock Out
	EPWM_CH0	I/O	MFP3	PWM channel0 output/capture input.
	I2C1_SCL	I/O	MFP8	I^2C1 clock pin.
	SPI0_SS	I/O	MFP9	SPI0 slave select pin.

Pin No.	Pin Name	Type	MFP*	Description
	SPI1_CLK	I/O	MFPA	SPI1 serial clock pin
	UART1_TXD	O	MFPB	Data transmitter output pin for UART1.
20	V_{SS}	A	MFP0	Ground pin for digital circuit.

Table 4.3-2 QFN20 Pin Description

4.3.3 GPIO Multi-function Pin Summary

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFP)

PA.0 MFP0 means SYS_GPA_MFP[3:0]=0x0.

PA.4 MFP5 means SYS_GPA_MFP[19:16]=0x5.

Group	Pin Name	GPIO	MFP*	Type	Description
ACMP0	ACMP0_P0	PB.0	MFP4	A	Comparator0 positive input pin.
	ACMP0_P1	PB.1	MFP4	A	Comparator0 positive input pin.
	ACMP0_P2	PB.2	MFP4	A	Comparator0 positive input pin.
	ACMP0_N	PB.4	MFP4	A	Comparator0 negative input pin.
	ACMP0_P3	PC.1	MFP4	A	Comparator0 positive input pin.
	ACMP0_O	PA.5	MFP4	O	Comparator0 output pin.
ACMP1	ACMP1_P1	PC.1	MFP5	A	Comparator1 positive input pin.
	ACMP1_N	PB.3	MFP5	A	Comparator1 negative input pin.
	ACMP1_O	PC.3	MPF5	O	Comparator1 output pin.
	ACMP1_P2	PD.1	MFP5	A	Comparator1 positive input pin.
	ACMP1_P0	PC.0	MFP5	A	Comparator1 positive input pin.
ADC0	ADC0_CH0	PB.0	MFP2	A	ADC0 analog input channel 0.
	ADC0_CH1	PB.1	MFP2	A	ADC0 analog input channel 1.
	ADC0_CH2	PB.2	MFP2	A	ADC0 analog input channel 2.
	ADC0_CH4	PC.1	MFP2	A	ADC0 analog input channel 4.
	ADC0_CH3	PC.0	MFP2	A	ADC0 analog input channel 3.
ADC1	ADC1_CH0	PB.4	MFP2	A	ADC1 analog input channel 0.
	ADC1_CH2	PC.2	MFP2	A	ADC1 analog input channel 2.
	ADC1_CH1	PD.2	MFP2	A	ADC1 analog input channel 1.
BPWM	BPWM_CH1	PB.2	MFP3	O	Basic PWM channel 1 output
	BPWM_CH0	PC.0	MFP3	O	Basic PWM channel 0 output
	BPWM_CH1	PD.3	MFP3	O	Basic PWM channel 1 output
	BPWM_CH0	PD.4	MFP3	O	Basic PWM channel 0 output
CCAP	CCAP_P1	PC.2	MFP7	I	Continuous Capture Input
	CCAP_P0	PD.2	MFP7	I	Continuous Capture Input
CLKO	CLKO	PA.0	MFP1	O	Clock output pin.
ECAP	ECAP_P0	PB.0	MFP7	I	Input capture channel 0
	ECAP_P1	PB.1	MFP7	I	Input capture channel 1
	ECAP_P2	PB.2	MFP7	I	Input capture channel 2

EPWM	BRAKE	PC.2	MFP3	I	EPWM brake pin.
	EPWM_CH5	PA.5	MFP3	O	Enhanced PWM output pin.
	EPWM_CH4	PA.4	MFP3	O	Enhanced PWM output pin.
	EPWM_CH3	PA.3	MFP3	O	Enhanced PWM output pin.
	EPWM_CH2	PA.2	MFP3	O	Enhanced PWM output pin.
	EPWM_CH1	PA.1	MFP3	O	Enhanced PWM output pin.
	EPWM_CH0	PA.0	MFP3	O	Enhanced PWM output pin.
I^2C	I2C1_SDA	PC.2	MFP8	I/O	I^2C1 data pin.
	I2C0_SDA	PD.2	MFP8	I/O	I^2C0 data pin.
	I2C0_SCL	PD.1	MFP8	I/O	I^2C0 clock pin.
	I2C1_SCL	PC.0	MFP8	I/O	I^2C1 clock pin.
	I2C0_SCL	PA.3	MFP8	I/O	I^2C0 clock pin.
	I2C0_SDA	PA.2	MFP8	I/O	I^2C0 data pin.
	I2C1_SDA	PA.1	MFP8	I/O	I^2C1 data pin.
	I2C1_SCL	PA.0	MFP8	I/O	I^2C1 clock pin.
ICE	ICE_DAT	PD.2	MFP1	I/O	Serial wired debugger data pin. (note 1)
	ICE_CLK	PD.1	MFP1	I	Serial wired debugger clock pin. (note 1)
nRESET	nRESET			I	External reset pin, internal pull-high.
PGA	PGA_I	PB.3	MFP6	A	PGA analog input pin.
	PGA_O	PC.3	MFP6	A	PGA analog output pin.
SPI0	SPI0_MOSI	PC.1	MFP9	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_MISO	PC.2	MFP9	I/O	SPI0 MISO (Master In, Slave Out) pin.
	SPI0_MOSI	PD.2	MFP9	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_CLK	PC.3	MFP9	I/O	SPI0 clock pin.
	SPI0_CLK	PD.1	MFP9	I/O	SPI0 clock pin.
	SPI0_SS	PC.0	MFP9	I	SPI0 slave selection pin.
	SPI0_CLK	PA.3	MFP9	I/O	SPI0 clock pin.
	SPI0_MOSI	PA.2	MFP9	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_MISO	PA.1	MFP9	I/O	SPI0 MISO (Master In, Slave Out) pin.
	SPI0_SS	PA.0	MFP9	I	SPI0 slave selection pin.
SPI1	SPI1_MISO	PC.1	MFPA	I/O	SPI1 MISO (Master In, Slave Out) pin
	SPI1_MOSI	PC.2	MFPA	I/O	SPI1 MOSI (Master Out, Slave In) pin.
	SPI1_MISO	PD.2	MFPA	I/O	SPI1 MISO (Master In, Slave Out) pin
	SPI1_SS	PC.3	MFPA	I/O	SPI1 Slave Select

	SPI1_SS	PD.1	MFPA	I/O	SPI1 Slave Select
	SPI1_CLK	PC.0	MFPA	I/O	SPI1 clock pin.
	SPI1_SS	PA.3	MFPA	I	SPI1 slave selection pin.
	SPI1_MISO	PA.2	MFPA	I/O	SPI1 MISO (Master In, Slave Out) pin.
	SPI1_MOSI	PA.1	MFPA	I/O	SPI1 MOSI (Master Out, Slave In) pin.
	SPI1_CLK	PA.0	MFPA	I/O	SPI1 clock pin.
STADC	STADC	PC.1	MFP3	I	External ADC trigger input pin.
TM0	TM0	PB.3	MFP7	I	Timer0 event counter input / toggle output
TM1	TM1	PB.4	MFP7	I	Timer1 event counter input / toggle output
UART0	UART0_RXD	PD.2	MFPB	I	UART0 data receiver input pin.
	UART0_TXD	PD.1	MFPB	O	UART0 data transmitter output pin.
	UART0_TXD	PA.3	MFPB	O	UART0 data transmitter output pin.
	UART0_RXD	PA.2	MFPB	I	UART0 data receiver input pin.
	UART0_TXD	PD.5	MFPB	O	UART0 data transmitter output pin.
	UART0_RXD	PD.6	MFPB	I	UART0 data receiver input pin.
UART1	UART1_RXD	PC.2	MFPB	I	UART1 data receiver input pin.
	UART1_TXD	PC.0	MFPB	O	UART1 data transmitter output pin.
	UART1_RXD	PA.1	MFPB	I	UART1 data receiver input pin.
	UART1_TXD	PA.0	MFPB	O	UART1 data transmitter output pin.
	UART1_TXD	PD.3	MFPB	O	UART1 data transmitter output pin.
	UART1_RXD	PD.4	MFPB	I	UART1 data receiver input pin.
XT	XT_OUT	PA.5	MPF1	A	External crystal output pin.
	XT_IN	PA.4	MFP1	A	External crystal input pin.

Table 4.3-2 TSSOP20 Multi-function Pin Summary

Note:

1. Do not leave the pins ICE_CLK and ICE_DAT in floating when MCU is in operatoin. User may refer to one of the following methods
    a. Add external pull-up or pull-low resistors at pins.
    b. Set the 2 pins in Quasi-mode and output high to be equivelant to internal pull high.
    c. Enable intenal pull-up by set PD_PHEN[2:1] = 11b.
    d. Be wired to other deivce without floating.

5 BLOCK DIAGRAM

5.1 NuMicro® NM1120 Block Diagram

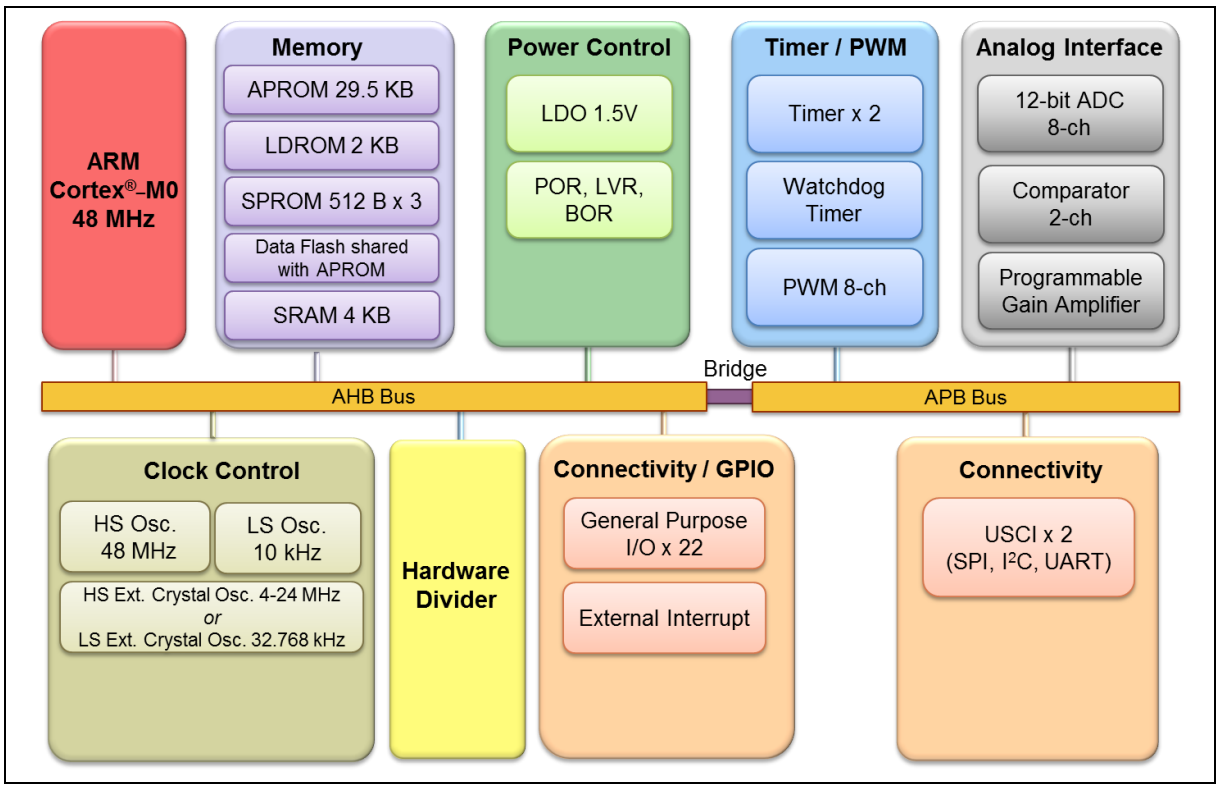


Figure 5.1-1 NuMicro® NM1120 Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

6.1.1 Overview

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes – Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6.1-1 shows the functional controller of processor.

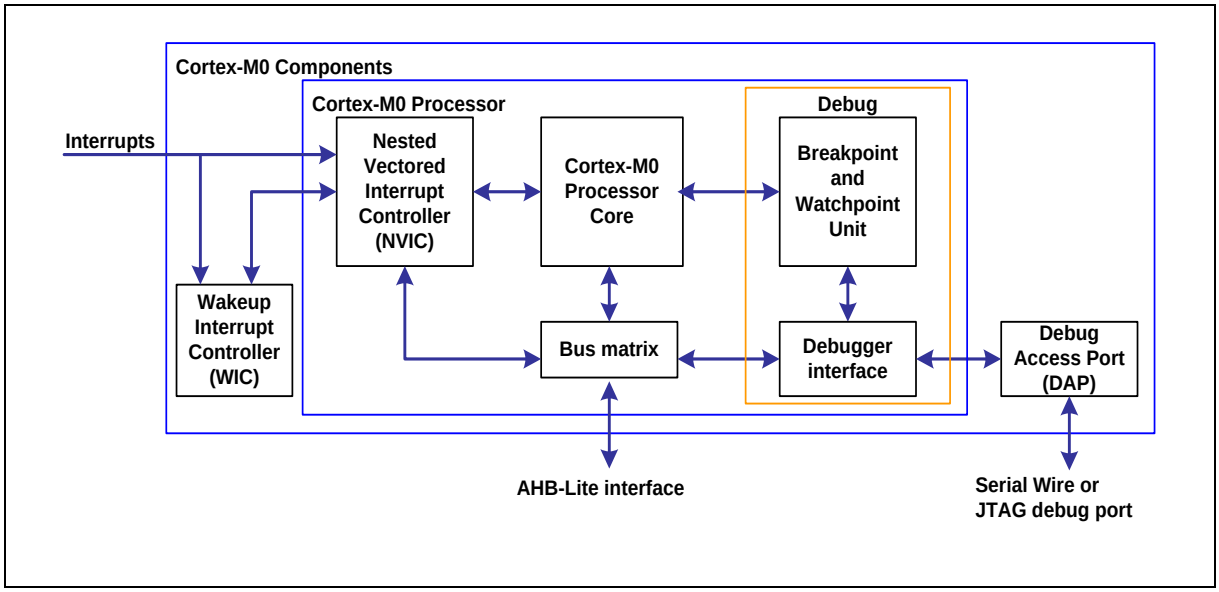


Figure 6.1-1 Functional Block Diagram

6.1.2 Features

The implemented device provides:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the

use of pure C functions as interrupt handlers

- Low Power Sleep mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature

- NVIC:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug support:
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset can reset chip through peripheral reset signals. Software reset can trigger reset through control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Timer Time-out Reset (WDT)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (SCS_AIRCR[2])
  - CPU Reset for Cortex®-M0 core Only by writing 1 to CPURST (SYS_IPRST0[1])

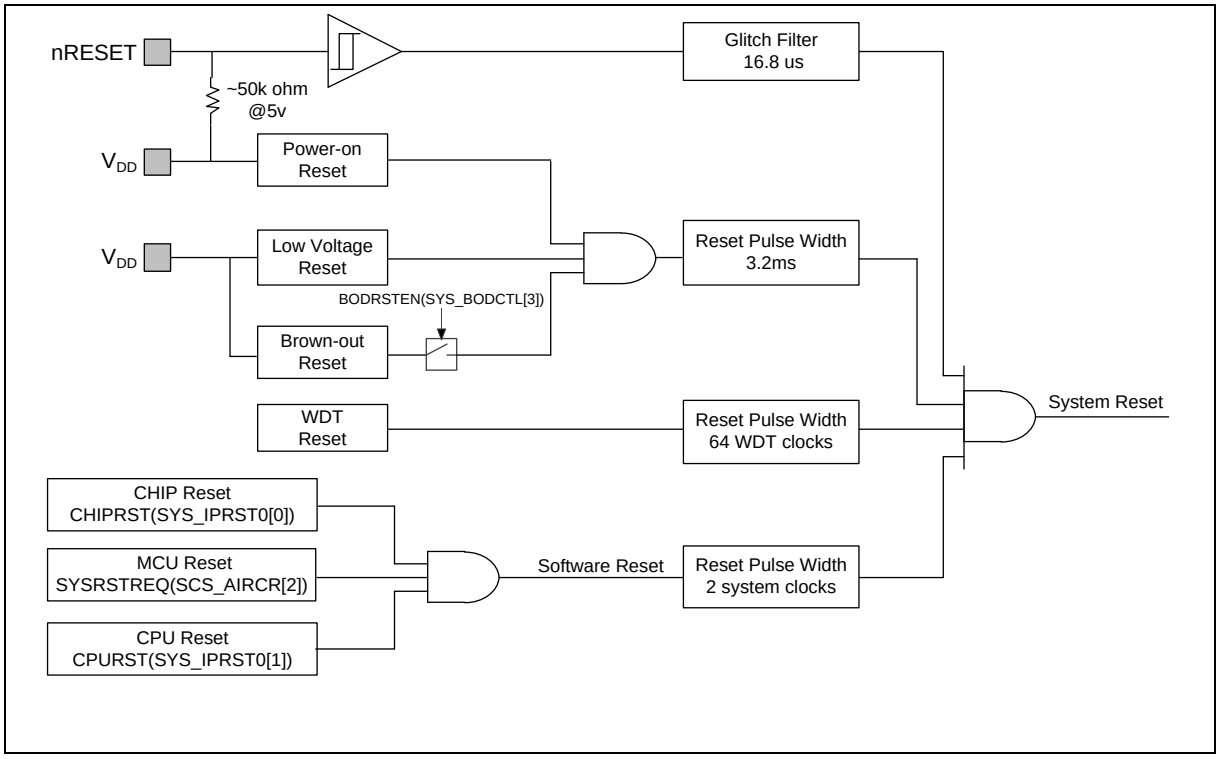


Figure 6.2-1 System Reset Resources

There are a total of 9 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M0 only; the other reset sources will reset Cortex®-M0 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-5.

Reset Sources / Register	POR	nRESET	WDT	LVR	BOD	CHIP	MCU	CPU
SYS_RSTSTS	0x001	Bit 1 = 1	Bit 2 = 1	0x001	Bit 4 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[3:1])								
BODRSTEN (SYS_BODCTL[4])								
XTLEN (CLK_PWRCTL[1:0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	0x1	-	-
HCLKSEL	0x8	0x8	0x8	0x8	0x8	0x8	0x8	-

(CLK_CLKSEL0[1:0])								
WDTSEL **(CLK_CLKSEL1[1:0])**	0x3	0x3	-	-	-	-	-	-
XLTSTB **(CLK_STATUS[0])**	0x0	-	-	-	-	-	-	-
LIRCSTB **(CLK_STATUS[3])**	0x0							
HIRCSTB **(CLK_STATUS[4])**	0x0	-	-	-	-	-	-	-
CLKSFAIL **(CLK_STATUS[7])**	0x0	0x0	-	-	-	-	-	-
WDT_CTL	0x0700	0x0700	0x0700	0x0700	0x0700	0x0700	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-	-
BS **(FMC_ISPCTL[1])** **ISPEN** **(FMC_ISPCTL[16])**	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
FMC_DFBA	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	-
CBS **(FMC_ISPSTS[2:1])**	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
VECMAP **(FMC_ISPSTS[20:9])**	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value							
FMC Registers	Reset Value							
Note: '-' means that the value of register keeps original setting.								

Table 6.2-1 Reset Value of Registers

6.2.3 Power Modes and Wake-up Sources

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-2 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	WDT, I²C, Timer, UART, SPI, ACMP, BOD and GPIO
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-2 Power Mode Difference Table

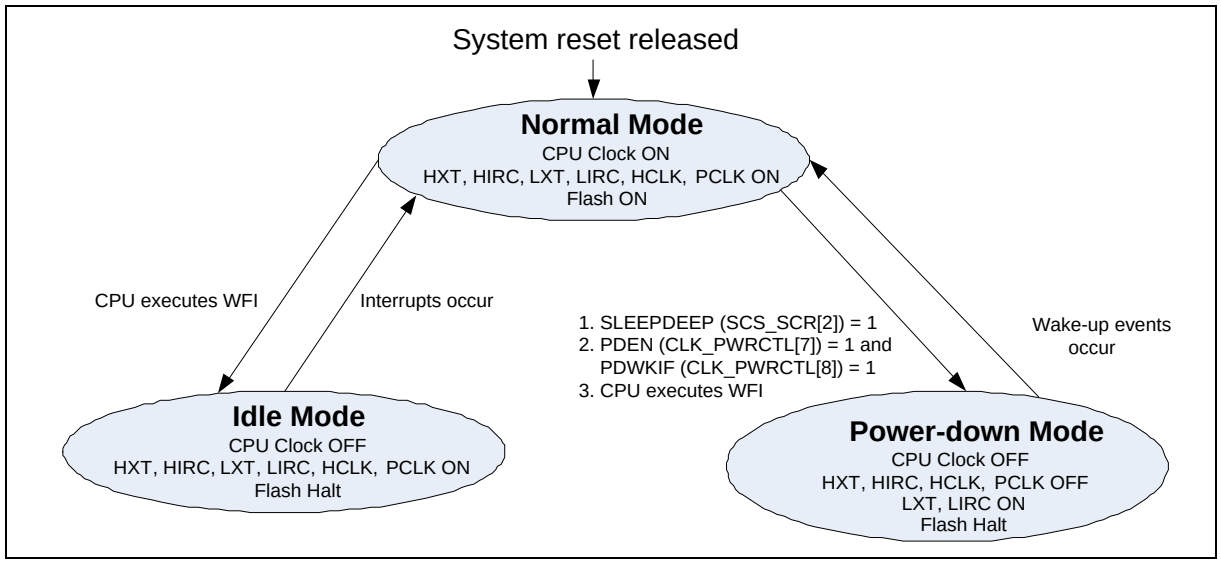


Figure 6.2-2 Power Mode State Machine

1. LXT (32768 Hz XTL) ON or OFF depends on SW setting in run mode.
2. LIRC (10 kHz OSC) ON or OFF depends on S/W setting in run mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.

	Normal Mode	Idle Mode	Power-Down Mode
HXT (4~20 MHz XTL)	ON	ON	Halt
HIRC (48 MHz OSC)	ON	ON	Halt
LXT (32768 Hz XTL)	ON	ON	ON/OFF[1]
LIRC (10 kHz OSC)	ON	ON	ON/OFF[2]
LDO	ON	ON	ON
CPU	ON	Halt	Halt
HCLK/PCLK	ON	ON	Halt
SRAM retention	ON	ON	ON
FLASH	ON	ON	Halt
GPIO	ON	ON	Halt
TIMER	ON	ON	ON/OFF[3]
BPWM	ON	ON	Halt
EPWM	ON	ON	Halt
WDT	ON	ON	ON/OFF[4]
USCI	ON	ON	Halt
ADC	ON	ON	Halt
ACMP	ON	ON	Halt
ECAP	ON	ON	Halt
HDIV	ON	ON	Halt
PGA	ON	ON	Halt

Table 6.2-3 Clocks in Power Modes

Wake-up sources in Power-down mode:

WDT, I²C, Timer, UART, SPI, BOD, ACMP and GPIO

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-4 lists the condition about how to enter Power-down mode again for each peripheral.

Note for BOD vs Power-down:

When the power-down mode is entered to save power consuming, the reference voltage of BOD(Brown-out Detection) will be disabled for saving power, therefore the BOD may incorrectly wake-up power down(if BOD interrupt is enabled) or trigger CPU reset(if BOR, brown-out reset, is enabled). It is a BOD function limitation in Power-down mode.

Recommended workaround for using BOD and power-down:

Please make sure that the BOD is disabled before entering Power-down mode. When the chip leaves Power-down mode, the BOD can be enabled again.

*User needs to wait this condition before setting PDEN (CLK_PWRCTL[7]) and execute WFI to enter

Power-down mode.

Wake-Up Source	Wake-Up Condition	System Can Enter Power-Down Mode Again Condition*
BOD	Brown-Out Detector Interrupt	After software writes 1 to clear SYS_BODCTL[BODIF].
GPIO	GPIO Interrupt	After software write 1 to clear the Px_INTSRC[n] bit.
TIMER	Timer Interrupt	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
WDT	WDT Interrupt	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
USCI UART	Incoming data wake-up	After software writes 1 to clear WKF (UUART_WKSTS[0]).
USCI SPI	SS transaction wake-up	After software writes 1 to clear WKF (USPI_WKSTS[0]).
USCI I^2C	Data toggle	After software writes 1 to clear WKF (UI2C_WKSTS[0]).
	Address match	After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], then writes 1 to clear WKF (UI2C_WKSTS[0]).
ACMP	Comparator Power-down Wake-Up Interrupt	After software writes 1 to clear ACMPF0 (ACMP_STATUS[0]) and ACMPF1 (ACMP_STATUS[1]).

Table 6.2-4 Condition of Entering Power-down Mode Again

6.2.4 System Power Architecture

In this chip, the power distribution is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation. AV_{DD} must be equal to V_{DD} to avoid leakage current.
- Digital power from V_{DD} and V_{SS} supplies power to the I/O pins and internal regulator which provides a fixed 1.5V power for digital operation.
- A built-in capacitor for internal voltage regulator

The output of internal voltage regulator, LDO, does not require an external capacitor and doesn't bond out to external pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 6.2-3 shows the power distribution of the NM1120 series.

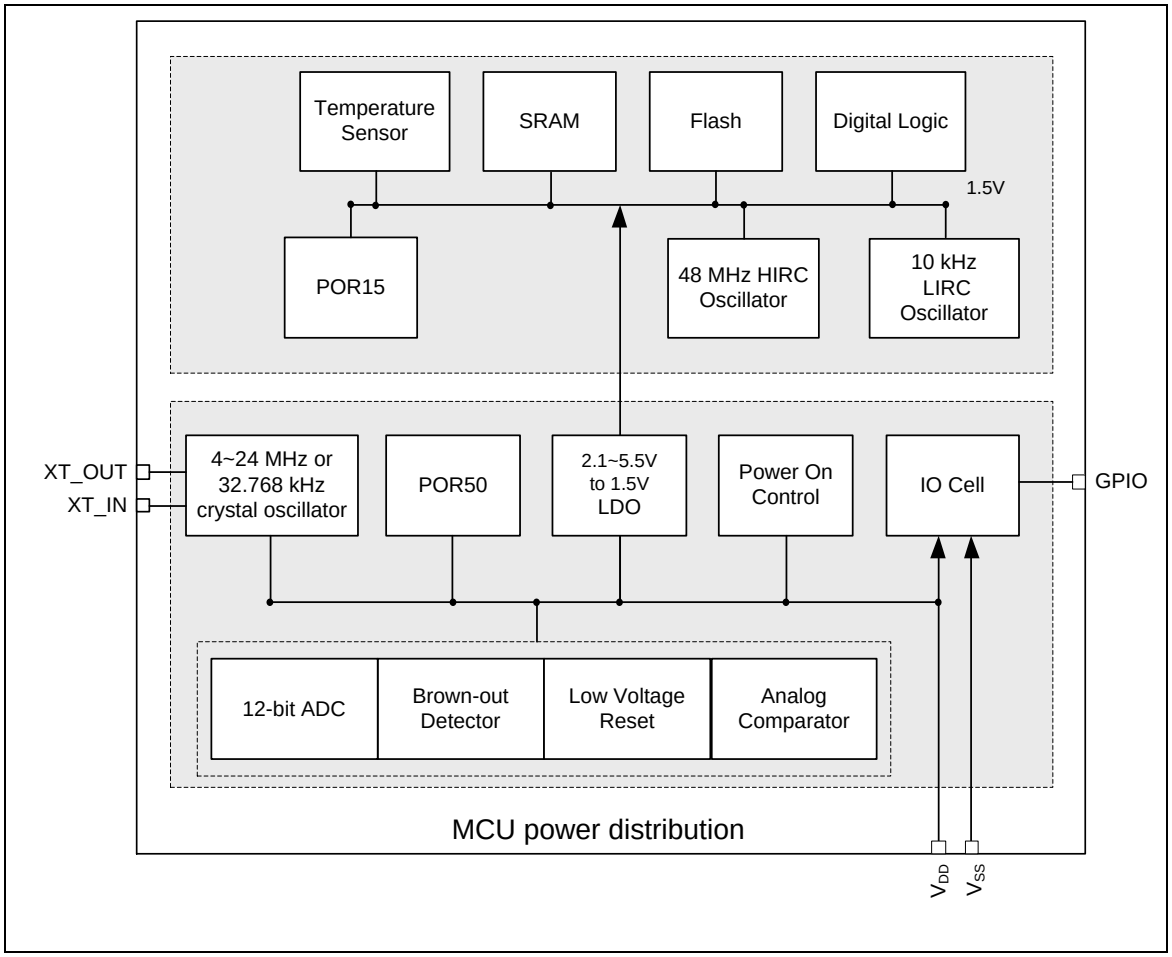


Figure 6.2-3 NuMicro® NM1120 Series Power Architecture Diagram

6.2.5 System Memory Mapping

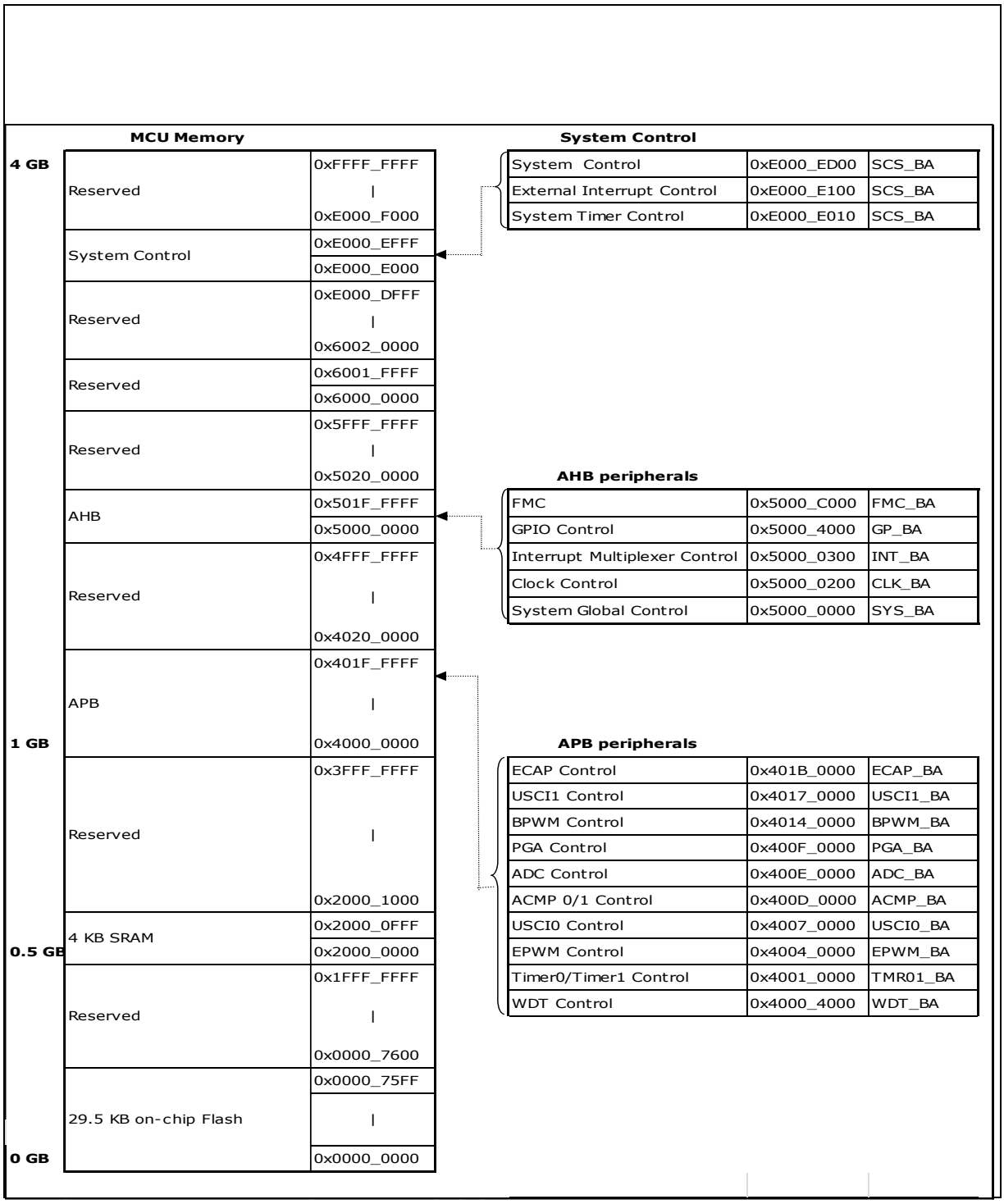


Table 6.2-5 Memory Mapping Table

6.2.6 Register Protection

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

After the protection is disabled, user can check REGLCTL (SYS_REGLCTL [0]), “1” is protection disable, “0” is protection enable. Then user can update the target protected register value and then write any data to SYS_REGLCTL to enable register protection.

The protected registers are listed in Table 6.2-6.

Register	Bit	Description
SYS_IPRST0	[1] CPURST	Processor Core One-shot Reset (Write Protect)
	[0] CHIPRST	Chip One-shot Reset (Write Protect)
SYS_BODCTL	[15] LVREN	Low Voltage Reset Enable Control (Write Protect)
	[6] BODLPM	Brown-out Detector Low Power Mode (Write Protect)
	[4] BODRSTEN	Brown-out Reset Enable Control (Write Protect)
	[3:1] BODVL	Brown-out Detector Threshold Voltage Selection (Write Protect)
	[0] BODEN	Brown-out Detector Enable Control (Write Protect)
SYS_PORCTL	[15:0] POROFF	Power-on Reset Enable Control (Write Protect)
INT_NMICTL	[8] NMISELEN	NMI Interrupt Enable Control (Write Protected)
CLK_PWRCTL	[11:10] HXTGAIN	HXT Gain Control (Write Protect)
	[7] PDEN	System Power-down Enable Control (Write Protect)
	[5] PDWKIEN	Power-down Mode Wake-up Interrupt Enable Control (Write Protect)
	[4] PDWKDLY	Wake-up Delay Counter Enable Control (Write Protect)
	[3] LIRCEN	LIRC Enable Control (Write Protect)
	[2] HIRCEN	HIRC Enable Control (Write Protect)
	[1:0] XTLEN	XTL Enable Control (Write Protect)
CLK_APBCLK	[0] WDTCKEN	Watchdog Timer Clock Enable Control (Write Protect)
CLK_CLKSEL0	[4:3] STCLKSEL	Cortex®-M0 SysTick Clock Source Selection (Write Protect)
	[1:0] HCLKSEL	HCLK Clock Source Selection (Write Protect)
CLK_CLKSEL1	[1:0] WDTSEL	Watchdog Timer Clock Source Selection (Write Protect)
FMC_ISPCTL	[6] ISPFF	ISP Fail Flag (Write Protect)
	[5] LDUEN	LDROM Update Enable Control (Write Protect)
	[4] CFGUEN	CONFIG Update Enable Control (Write Protect)

	[3] APUEN	APROM Update Enable Control (Write Protect)
	[2] SPUEN	SPROM Update Enable Control (Write Protect)
	[1] BS	Boot Select (Write Protect)
	[0] ISPEN	ISP Enable Control (Write Protect)
FMC_ISPTRG	[0] ISPGO	ISP Start Trigger (Write Protect)
FMC_ISPSTS	[6] ISPFF	ISP Fail Flag (Write Protect)
TIMER0_CTL	[31] ICEDEBUG	ICE Debug Mode Acknowledge Disable Control (Write Protect)
TIMER1_CTL	[31] ICEDEBUG	ICE Debug Mode Acknowledge Disable Control (Write Protect)
WDT_CTL	[31] ICEDEBUG	ICE Debug Mode Acknowledge Disable Control (Write Protect)
	[7] WDTEN	Watchdog Timer Enable Control (Write Protect)
	[6] INTEN	Watchdog Timer Time-out Interrupt Enable Control (Write Protect)
	[4] WKEN	Watchdog Timer Time-out Wake-up Function Control (Write Protect)
	[1] RSTEN	Watchdog Timer Time-out Reset Enable Control (Write Protect)
	[0] RSTCNT	Reset Watchdog Timer Up Counter (Write Protect)

Table 6.2-6 Protected Registers

6.2.7 Memory Organization

6.2.7.1 Overview

The NuMicro® NM1120 series provides 4G-byte addressing space. The addressing space assigned to each on-chip controllers is shown in Figure 6.2-4. The detailed register definition, addressing space, and programming details will be described in the following sections for each on-chip peripheral. The NM1120 series only supports little-endian data format.

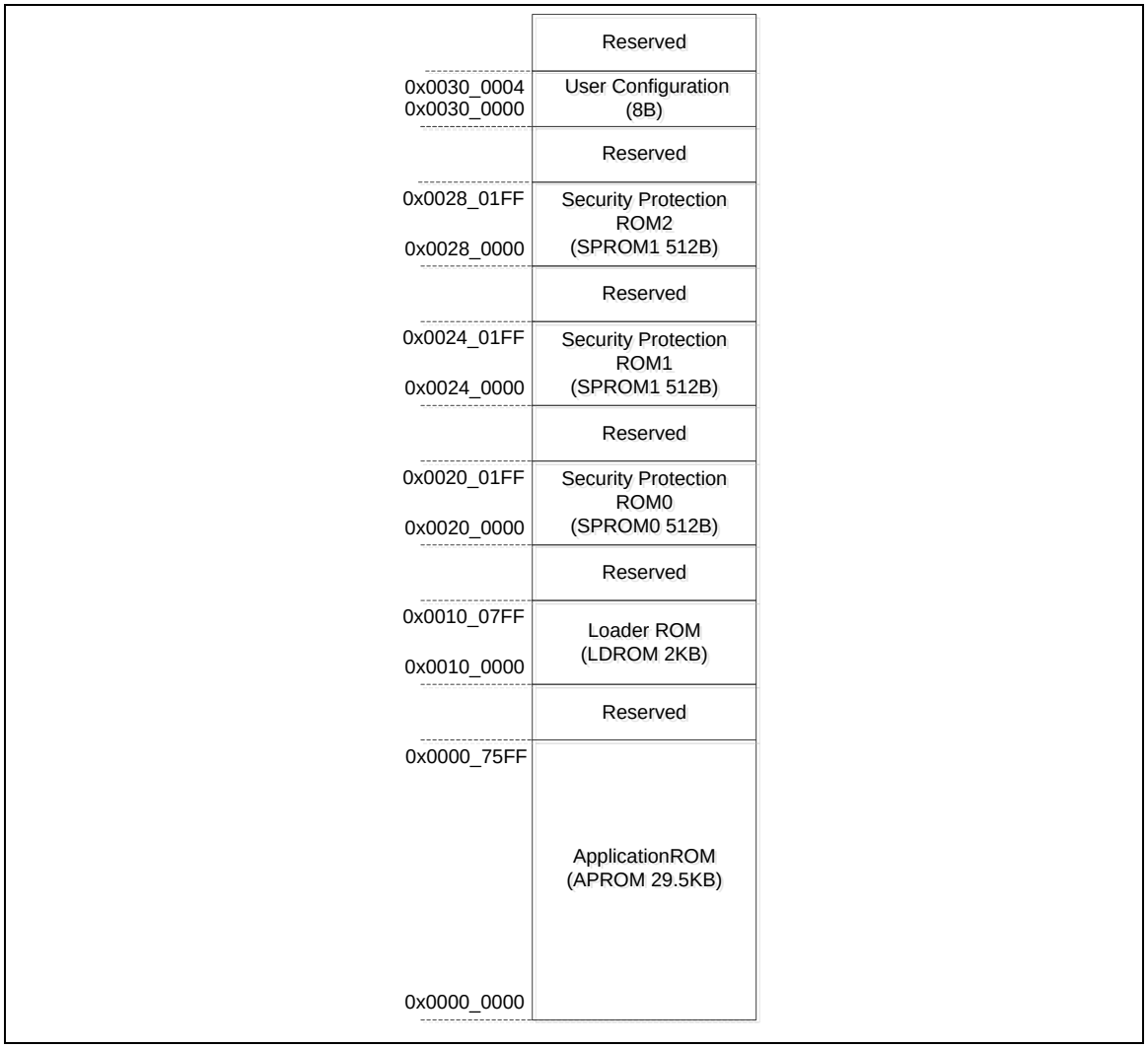


Figure 6.2-4 NuMicro® NM1120 Flash, Security and Configuration Map

6.2.8 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit cleared-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, for example:

An RTOS tick timer fires at a programmable rate (for example 100Hz) and invokes a SysTick routine.

A high-speed alarm timer uses Core clock.

A variable rate alarm or signal timer – the duration range is dependent on the reference clock used and the dynamic range of the counter.

A simple counter can be used by software to measure task completion time.

An internal Clock Source control based on missing/meeting durations. The COUNTFLAG bit-field in the control and status register can be used to determine if an action completed within a set duration, as part of a dynamic clock management control loop.

When enabled, the timer will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock edge, and then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on read.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.2.9 Nested Vectored Interrupt Control (NVIC)

6.2.9.1 Overview

The Cortex®-M0 CPU provides an interrupt controller as an integral part of the exception mode, named as “Nested Vectored Interrupt Controller (NVIC)”, which is closely coupled to the processor core and provides following features.

6.2.9.2 Features

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority change
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in “Handler Mode”. This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one’s priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the Interrupt Service Routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers “PC, PSR, LR, R0~R3, R12” to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports “Tail Chaining” which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports “Late Arrival” which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

6.2.10 System Control Registers

Key control and status features of Cortex®-M0 are managed centrally in a System Control Block within the System Control Registers.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when the Cortex®-M0 core executes the WFI instruction only if the PDEN (CLK_PWRCTL[7]) bit set to 1. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to exit Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 48 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. Figure 6.3-1 shows the clock generator and the overview of the clock source control.

6.3.2 Clock Diagram

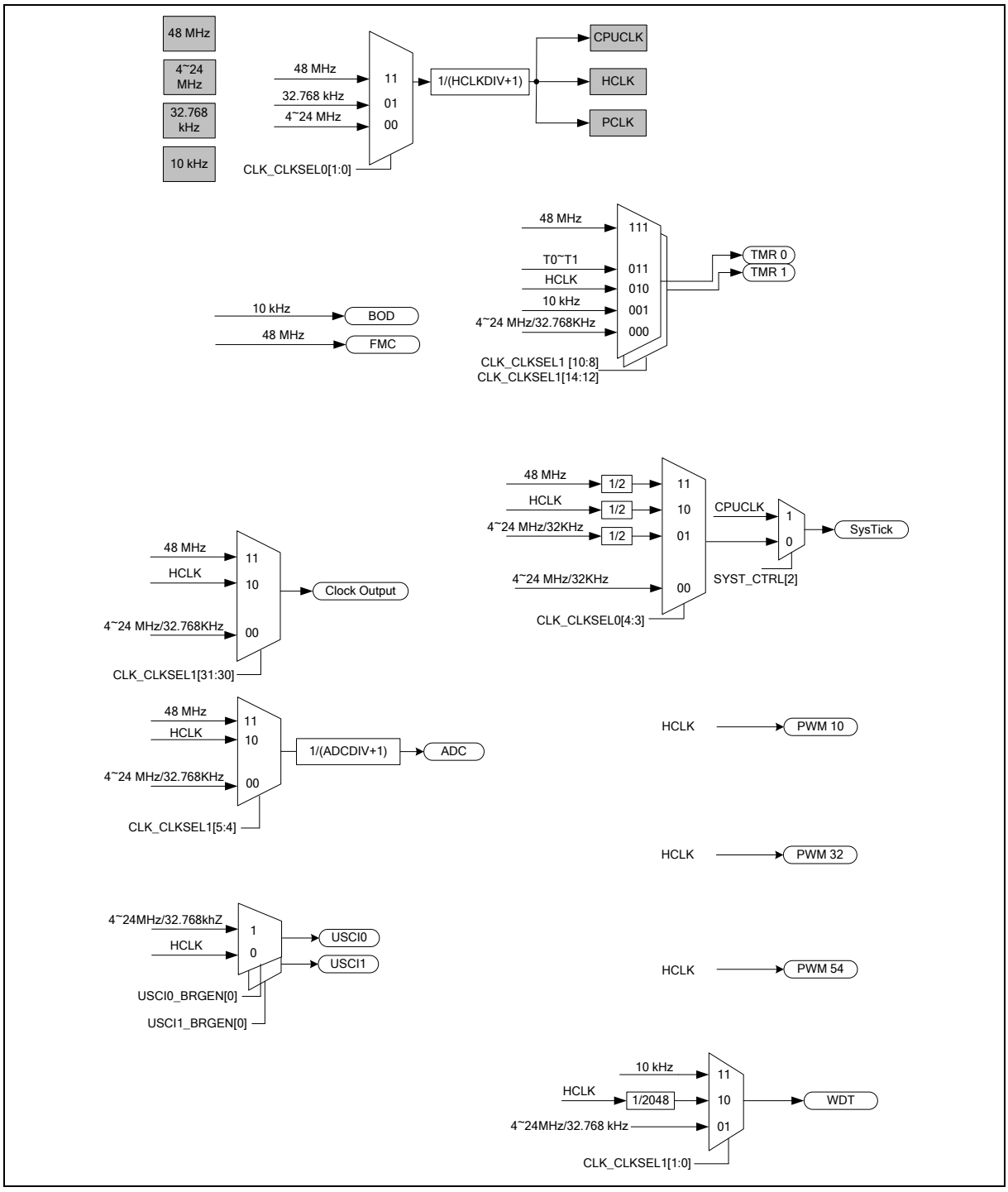


Figure 6.3-1 Clock Generator Global View Diagram

6.3.3 Clock Generator

The clock generator consists of 4 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- 48 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

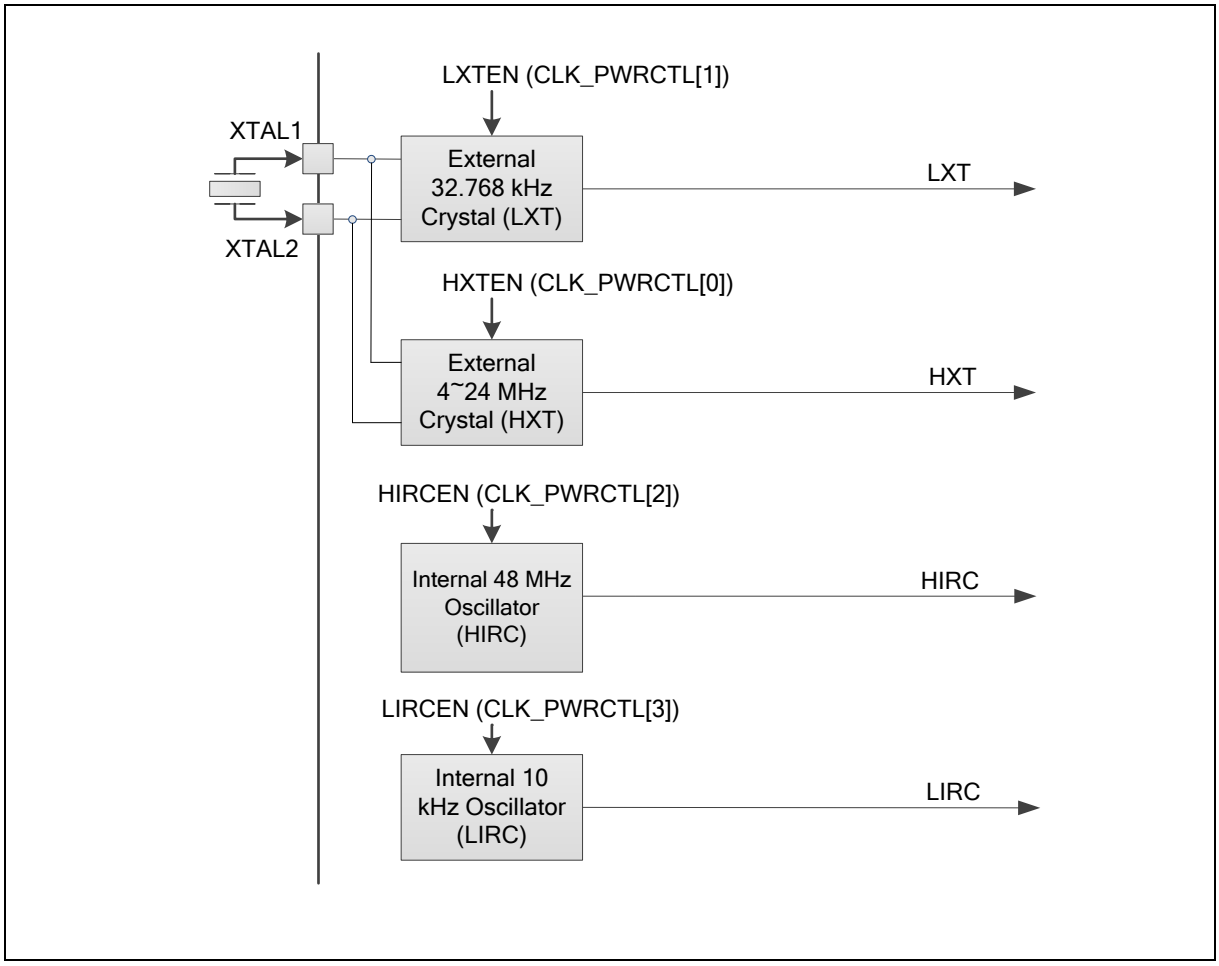


Figure 6.3-2 Clock Generator Block Diagram

The external crystal oscillator and two capacitors are connected to the pad “XT_IN” and pad “XT_OUT”. The capacitance value of the two capacitors may be changed for differential crystal oscillator from different vender. The load capacitance values and resistance values must be adjusted according to the selected oscillator. The recommended load capacitance values and resistance values as

Crystal Oscillator	Capacitance Values	Resistance Values
12 MHz	C1:20pF , C2:20pF	Hi-Z (Build in Chip)
32.768 kHz	C1:20pF , C2:20oF	Hi-Z (Build in Chip)

Table 6.3-1 Recommended Load Capacitance Values and Resistance Values

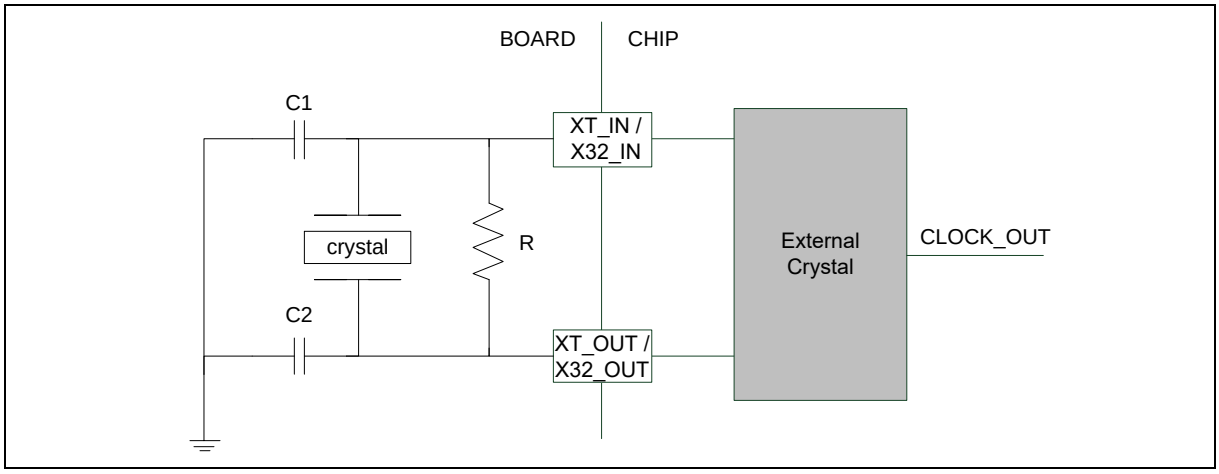


Figure 6.3-3 Crystal Oscillator Circuit

6.3.4 System Clock and SysTick Clock

The system clock has three clock sources which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[1:0]). The block diagram is shown in Figure 6.3-4.

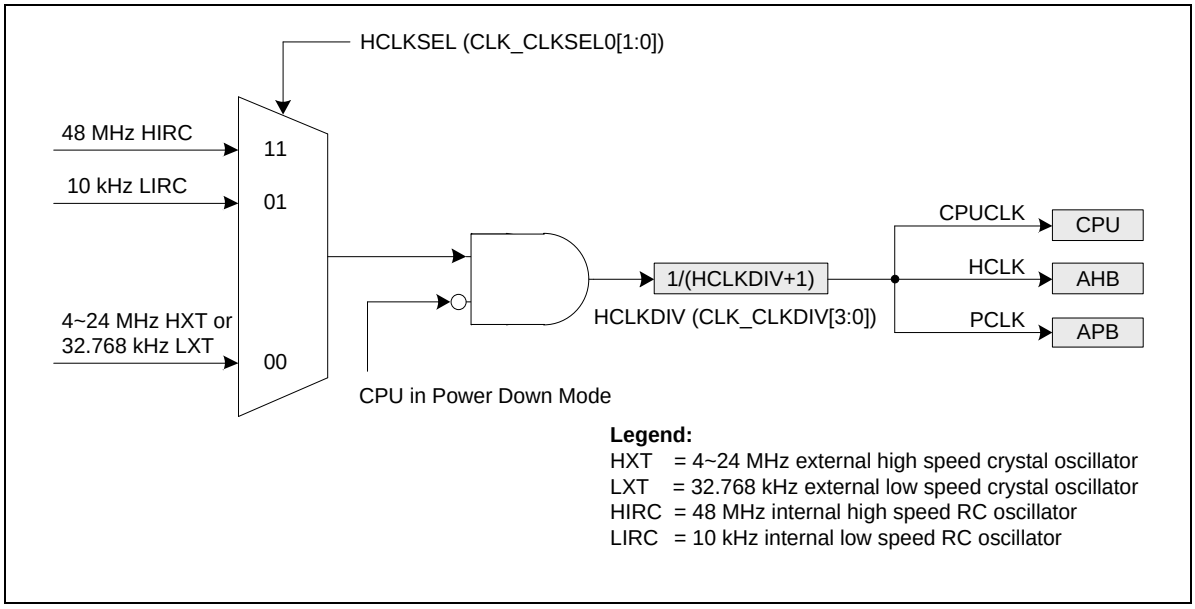


Figure 6.3-4 System Clock Block Diagram

The clock source of SysTick in the Cortex®-M0 core can use CPU clock or external clock (SYST_CTL[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[4:3]). The block diagram is shown in Figure 6.3-5.

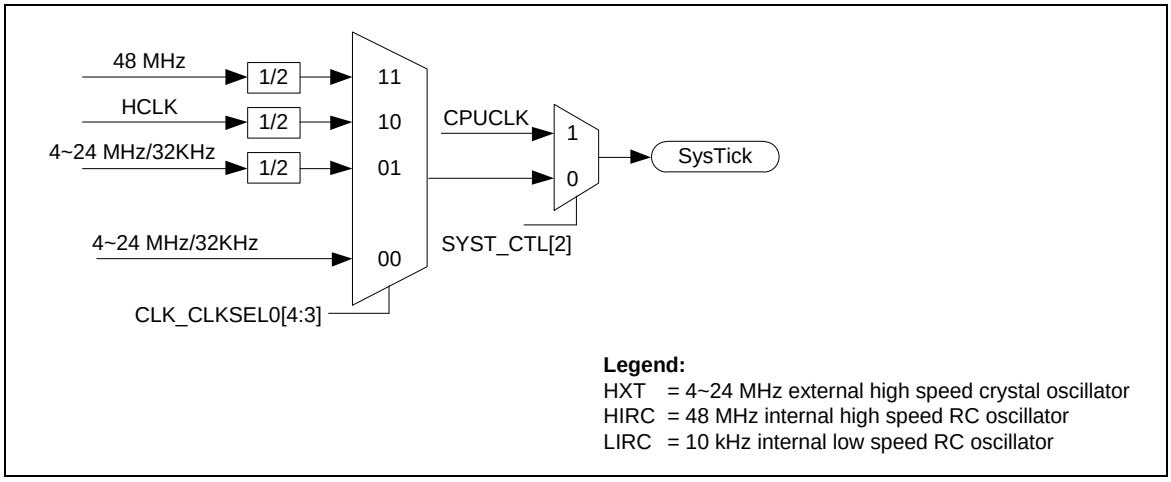


Figure 6.3-5 SysTick Clock Control Block Diagram

6.3.5 AHB Clock Source Selection

The clock source of ISP is from AHB clock (HCLK). Please refer to register CLK_AHBCLK.

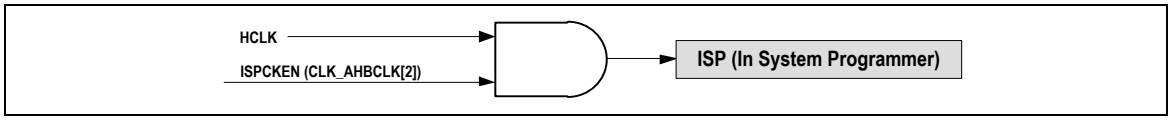


Figure 6.3-6 AHB Clock Source for HCLK

6.3.6 Peripherals Clock Source Selection

The peripheral clock has different clock source switch settings depending on different peripherals. Please refer to the CLK_CLKSEL1 and CLK_APBCLK register description in section **錯誤! 找不到參照來源。**.

6.3.7 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
- 10 kHz internal low speed oscillator (LIRC) clock
- 32.768 kHz external low speed crystal oscillator (LXT) clock (If PDLXT = 1 and XTLEN[1:0] = 10)
- Peripherals Clock (When 10 kHz low speed oscillator is adopted as clock source)
  - Watchdog Clock
  - Timer 0/1 Clock

6.3.8 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to the CLKO pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $F_{out} = F_{in}/2^{(N+1)}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

if DIV1EN(CLK_CLKOCTL[5]) set to 1, the frequency divider clock will bypass power-of-2 frequency divider. The frequency divider clock will be output to CLKO pin directly.

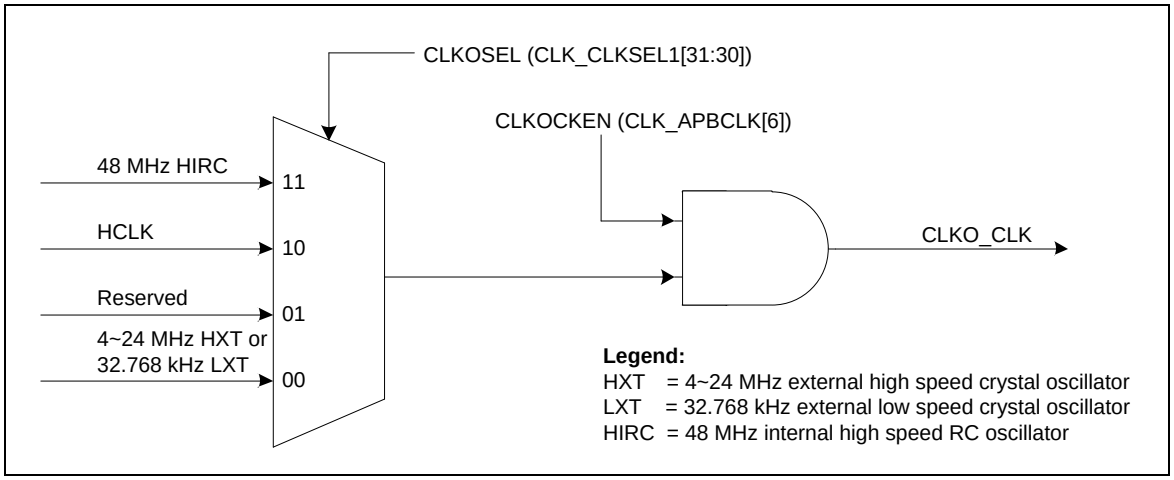


Figure 6.3-7 Clock Source of Frequency Divider

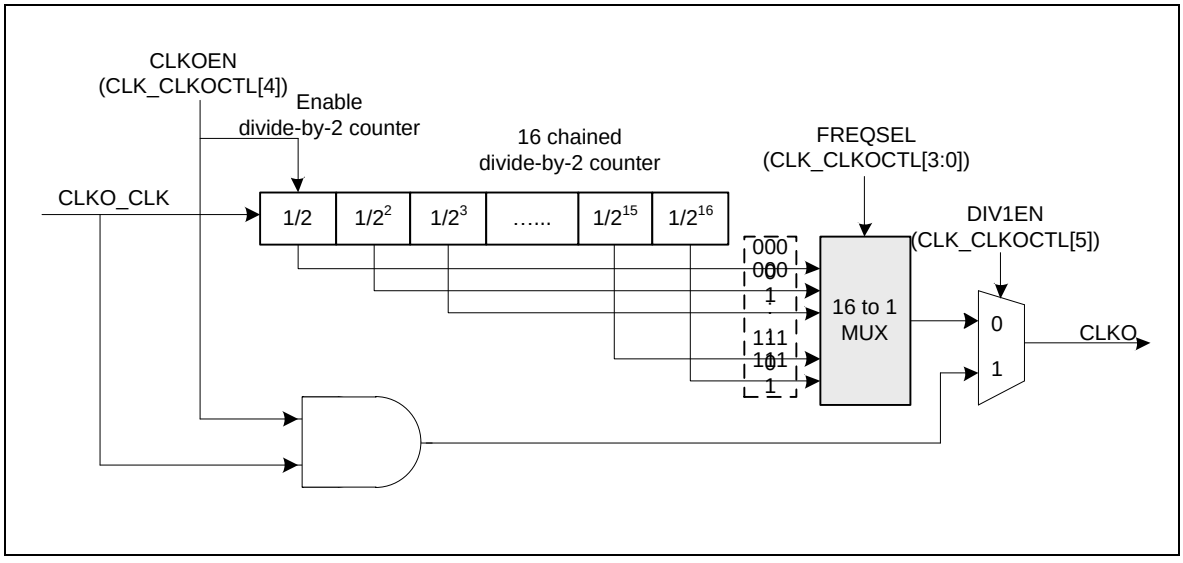


Figure 6.3-8 Block Diagram of Frequency Divider

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The NM1120 series is equipped with 29.5 Kbytes on chip embedded Flash EPROM for application program memory (APROM) that can be updated through ISP procedure. In System Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip powered on Cortex®-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, the NM1120 series also provides Data Flash Region, where the Data Flash is shared with original program memory and its start address is configurable and defined by user in Config1. The Data Flash size is defined by user depending on the application request. Security program memory (SPROM) provides user to protect any program code within SPROM.

6.4.2 Features

- Running up to 48 MHz with one wait state and 24 MHz without wait state for discontinuous address read access
- 29.5 Kbytes application program memory (APROM)
- 2 Kbytes in system programming (ISP) loader program memory (LDROM)
- Programmable Data Flash start address and memory size with 512 bytes page erase unit
- Three 512 bytes security program memory (SPROM)
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory.

6.4.3 Block Diagram

The flash memory controller consist of AHB slave interface, ISP control logic, writer interface and flash macro interface timing control logic. The block diagram of flash memory controller is shown in Figure 6.4-1:

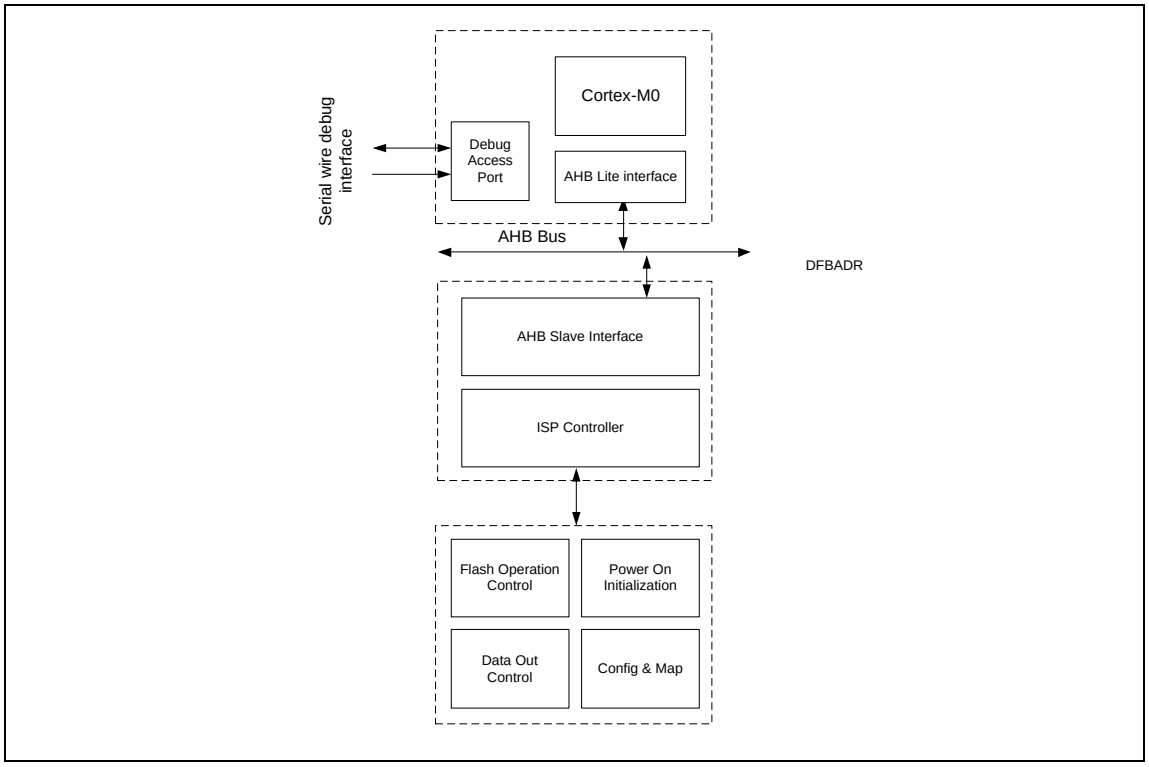


Figure 6.4-1 Flash Memory Control Block Diagram

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

The NM1120 series has up to 22 General Purpose I/O pins and one input pin. These pins could be shared with other functions depending on the chip configuration. 22 pins are arranged in 4 ports named as PA, PB, PC, and PD. Each of the 22 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOIN (CONFIG0[10]).

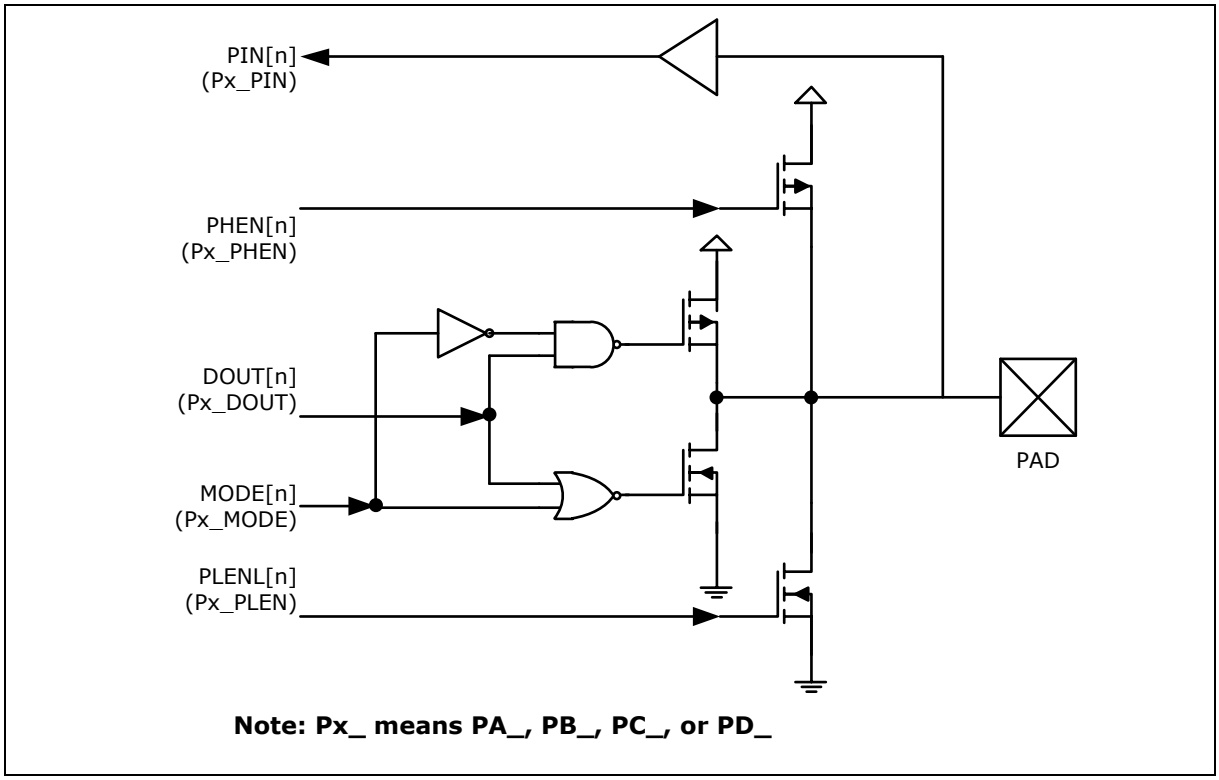


Figure 6.5-1 I/O Pin Block Diagram

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOIN = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOIN = 1, all GPIO pins in input mode after chip reset
- All supports the pull-up and pull-low resistor enabled in four I/O modes
- Enabling the pin interrupt function will also enable the wake-up function

6.6 Timer Controller (TIMER)

6.6.1 Overview

The Timer Controller includes two 32-bit timers, TIMER0 ~ TIMER1, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.6.2 Features

- Supports two sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Supports independent clock source for each channel (TMR0_CLK, TMR1_CLK)
- Supports four timer counting modes: one-shot, periodic, toggle and continuous counting
- Time-out period = (period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit CMPDAT)
- Supports maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}); T is the period of timer clock
- 24-bit up counter value is readable through TIMERx_CNT (Timer Data Register)
- Supports event counting function to count the event from external pin (TM0, TM1)
- Supports internal capture triggered while internal ACMP output signal transition
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated

6.7 Enhanced Input Capture Timer (ECAP)

6.7.1 Overview

This device provides an Input Capture Timer/Counter which capture function can detect the digital edge changed signal at channel inputs. This unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

6.7.2 Features

- Supports the interrupt function
- 24-bit Input Capture up-counting timer/counter
- Supports noise filter in front end of input ports
- Edge detector with three options
  - Rising edge detection
  - Falling edge detection
  - Both edge detection
- Each input channel is supported with one capture counter hold register
- Captured event reset/reload capture counter option
- Supports the compare-match function

6.8 Enhanced PWM Generator (EPWM)

6.8.1 Overview

The NM1120 has built in one PWM unit which is specially designed for motor driving control applications. The PWM unit supports six PWM generators which can be configured as six independent PWM outputs, PWM0~PWM5, or as three complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5) with three programmable dead-zone generators.

Every complementary PWM pairs share one clock divider providing nine divided frequencies (1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256) for each channel. Each PWM output shares one 16-bit counter for PWM period control, and 16-bit comparators for PWM duty control. The six PWM generators provide fourteen independent PWM interrupt flags which are set by hardware when the corresponding PWM period counter comparison matched period and duty. Each PWM interrupt source with its corresponding enable bit can request PWM interrupt. The PWM generators can be configured as One-shot mode to produce only one PWM cycle signal or Auto-reload mode to output PWM waveform continuously.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period up counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers, the updated value will be loaded into the 16-bit counter/comparator at the end of current period. The double buffering feature avoids glitch at PWM outputs.

Besides PWM, Motor controlling also need Timer, ACMP and ADC to work together. To control motor more precisely, some registers are provided to configure not only PWM but also Timer, ADC and ACMP. By doing so, it can save more CPU time and control motor with ease especially in BLDC.

6.8.2 Features

- Supports one PWM clock timer and one 9 level Divider (1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256).
- Supports six independent 16-bit PWM duty control units with maximum six port pins:
  - Six independent PWM outputs – PWM0, PWM1, PWM2, PWM3, PWM4, and PWM5
  - Three complementary PWM pairs, with each pin in a pair mutually complement to each other and capable of programmable dead-zone insertion – (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5)
- Supports group function.
- Supports one-shot (only edge alignment mode) or auto-reload mode PWM
- Supports 16-bit resolution PWM counter
- Supports Edge-aligned and Center-aligned mode
- Supports Programmable dead-zone insertion between complementary paired PWMs
- Supports hardware fault brake protections
  - Two Interrupt source types:
    - one type is brake directed, and one type can resume from brake.
    - fault brake source:
      - BRK0: ACMP0, ACMP1, EADC and External pin (BRAKE).
      - BRK1: ACMP0, ACMP1, EADC and External pin (BRAKE).

- The PWM signals before polarity control stage are defined in the view of positive logic. The PWM ports is active high or active low are controlled by polarity control register.
- Supports independently falling CMPDAT matching, central matching (in Center-aligned mode), rising CMPDAT matching (in Center-aligned mode), period matching to trigger EADC conversion
- Supports ACMP output event trigger PWM to force PWM output at most one period low
- Supports interrupt accumulation function

6.9 Basic PWM Generator (BPWM)

6.9.1 Overview

The NM1120 series has one set of BPWM group supporting one set of PWM generator that can be configured as 2 independent PWM outputs, PWM20~PWM21, or as 1 complementary PWM pairs, (PWM20, PWM21) with programmable Dead-zone generators.

The PWM generator has one 8-bit pre-scalar, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM up/down-counters for PWM period control, two 16-bit comparators for PWM duty control and one dead-zone generator. The PWM generator provides two independent PWM interrupt flags which are set by hardware when the corresponding PWM period down counter reaches zero. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When DTCNT01(BPWM_CTL[4]) is set, PWM20 and PWM21 perform complementary; the paired PWM timing, period, duty and dead-time are determined by PWM0 timer and Dead-zone generator 0. Refer to **錯誤! 找不到參照來源。** for the architecture of Basic PWM Timers.

To prevent PWM driving output pin from glitches, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching zero. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches zero, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches zero, it is reloaded with BPWM Counter Register(BPWM_PERIODx, x=0,1) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches zero.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

6.9.2 Features

- One PWM generator which supports one 8-bit pre-scalar, one clock divider, two PWM timers (down counter), one dead-zone generator and two PWM outputs.
- Up to 16-bit resolution
- PWM Interrupt request synchronized with PWM period
- One-shot or Auto-reload mode PWM
- Edge-aligned type or Center-aligned type option

6.10 Watchdog Timer (WDT)

6.10.1 Overview

The Watchdog Timer is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, the Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.10.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval
- Selectable time-out interval (24 ~ 218) WDT_CLK cycle and the time-out interval period is 104 ms ~ 26.3168 s if WDT_CLK = 10 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports Watchdog Timer time-out wake-up function only if WDT clock source is selected as 10 kHz

6.11 USCI – Universal Serial Control Interface Controller

6.11.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

Note: For detailed USCI UART, I^2C and SPI information, please refer to section 6.12, 6.13 and 6.14.

6.11.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I^2C

6.12 USCI – UART Mode

6.12.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter being independent, frames can start at different points in time for transmission and reception.

The UART controller also provides the LIN function. There is incoming data to wake up the system.

6.12.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports programmable baud-rate generator
- Supports 9-Bit Data Transfer
- Supports LIN function
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports Wake-up function

6.13 USCI – SPI Mode

6.13.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI_CTL[2:0]) = 0x1.

The SPI protocol can operate as master or Slave mode by setting the SLAVE (USPI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in master and Slave mode are shown as Figure 6.13-1 and Figure 6.13-2.

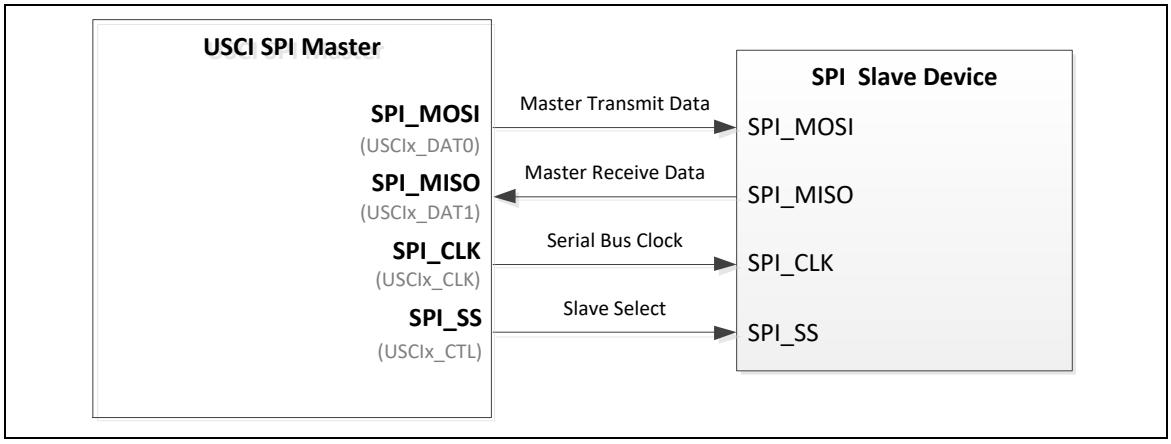


Figure 6.13-1 SPI Master Mode Application Block Diagram (x=0, 1)

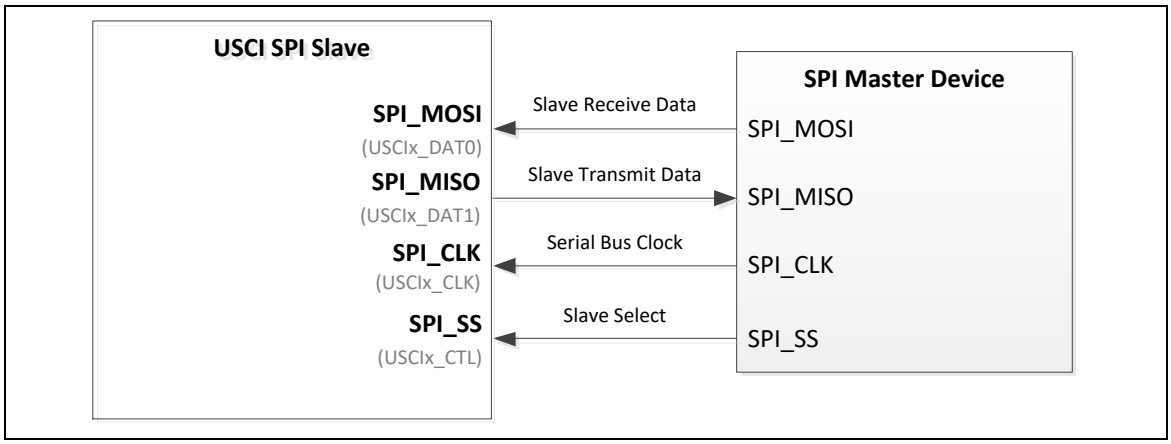


Figure 6.13-2 SPI Slave Mode Application Block Diagram (x=0, 1)

6.13.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master = f_{PCLK} / 2, Slave < f_{PCLK} / 5)
- Configurable bit length of a transfer word from 4 to 16-bit

- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence
- Supports Word Suspend function
- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode

6.14 USCI – I²C Mode

6.14.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6.14-1 for more detailed I²C BUS Timing.

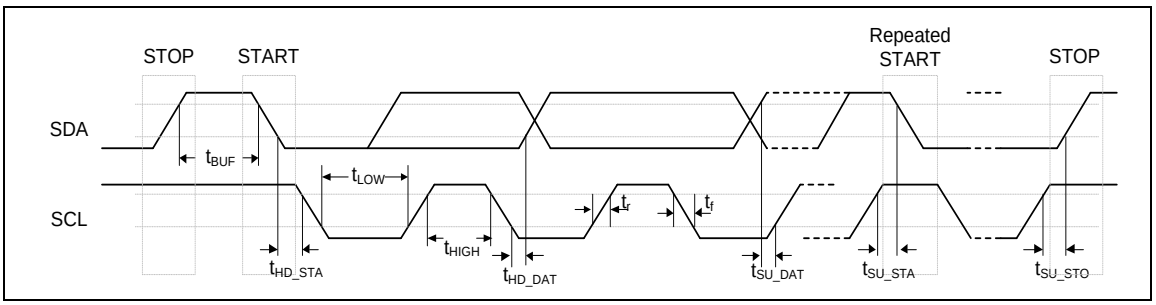


Figure 6.14-1 I²C Bus Timing

The device on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C mode is selected by FUNMODE (UI2C_CTL [2:0]) = 0100B. When this port is enabled, the USCI interfaces to the I²C bus via two pins: SDA and SCL. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

Note: A pull-up resistor is needed for I²C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I²C operation mode.

6.14.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports Power down wake-up by data toggle or address match
- Supports setup/hold time programmable

6.15 Hardware Divider (HDIV)

6.15.1 Overview

The hardware divider (HDIV) is useful to the high performance application. The hardware divider is a signed, integer divider with both quotient and remainder outputs.

6.15.2 Features

- Signed (two's complement) integer calculation
- 32-bit dividend with 16-bit divisor calculation capacity
- 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
- Divided by zero warning flag
- 6 HCLK clocks taken for one cycle calculation
- Write divisor to trigger calculation
- Waiting for calculation ready automatically when reading quotient and remainder

6.16 Analog to Digital Converter (ADC)

6.16.1 Overview

The NM1120 series contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with 8 single-end external input channels. The A/D converters can be started by software, external pin (STADC/PC.1) or PWM trigger.

6.16.1 Features

- Analog input voltage range: 0~V_{DD}.
- 12-bit resolution and 10-bit accuracy guaranteed.
- Up to 8 single-end analog input channels.
- ADC clock frequency up to 16MHz.
- Configurable ADC internal sampling time.

6.17 Analog Comparator (ACMP)

6.17.1 Overview

The NM1120 series contains two comparators which can be used in a number of different configurations. The comparator output is logic 1 when positive input greater than negative input, otherwise the output is 0. Each comparator can be configured to generate interrupt when the comparator output value changes.

6.17.2 Features

- Analog input voltage range: 0 ~ AV_{DD}
- Supports Hysteresis function
- Optional internal reference voltage source for each comparator negative input

6.18 Programmable Gain Amplifier (PGA)

6.18.1 Overview

The NM1120 series contains a programmable gain amplifier (PGA) which can be enabled through the PGAEN bit. User can measure the outputs of the programmable gain amplifier as the programmable gain amplifier output to the integrated A/D converter channel, where digital results can be taken. Furthermore, user can adjust gain to 1, 2, 3, 5, 7, 9, 11 and 13.

Note: The analog input port pins must be configured as input type before the PGA function is enabled.

6.18.2 Features

- Supports analog input voltage range: 0~ V_{DD}.
- Supports programmable gain: 1, 2, 3, 5, 7, 9, 11, 13
- Supports PGA output as input of ADC and ACMP

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}– V_{SS}	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} -0.3	V_{DD} +0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+105	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}	-	120	mA
I_{IO}	Maximum Current sunk by an I/O pin	-	35	mA
	Maximum Current sourced by an I/O pin	-	35	mA
	Maximum Current sunk by total I/O pins	-	100	mA
	Maximum Current sourced by total I/O pins	-	100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

7.2 DC Electrical Characteristics

(V_{DD} - V_{SS} = 2.1 ~ 5.5 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions			
V_{DD}	Operation voltage	2.1	-	5.5	V	V_{DD} = 2.1V ~ 5.5V up to 48 MHz			
V_{SS} / AV_{SS}	Power Ground	-0.3	-	-	V				
V_{LDO}	LDO Output Voltage		1.5		V				
V_{BG}	Band-gap Voltage[3]	1.14	1.20	1.26	V	V_{DD} = 3.0V ~ 5.5V, T_A = -40°C~105°C			
I_{DD5}	Operating Current Normal Run Mode HCLK = 48 MHz while(1){} Executed from Flash	-	9.7	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	X	48 MHz	V
I_{DD6}		-	7.4	-	mA	5.5V	X	48 MHz	X
I_{DD7}		-	9.7	-	mA	3V	X	48 MHz	V
I_{DD8}		-	7.4	-	mA	3V	X	48 MHz	X
I_{DD1}	Operating Current Normal Run Mode HCLK = 24 MHz while(1){} Executed from Flash	-	5.4	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	24 MHz	X	V
I_{DD2}		-	4.4	-	mA	5.5V	24 MHz	X	X
I_{DD3}		-	5.4	-	mA	3V	24 MHz	X	V
I_{DD4}		-	4.4	-	mA	3V	24 MHz	X	X
I_{DD9}	Operating Current Normal Run Mode HCLK = 16 MHz while(1){} Executed from Flash	-	3.7	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	16 MHz	X	V
I_{DD10}		-	3.0	-	mA	5.5V	16 MHz	X	X
I_{DD11}		-	3.7	-	mA	3V	16 MHz	X	V
I_{DD12}		-	3.1	-	mA	3V	16 MHz	X	X
I_{DD9}	Operating Current Normal Run Mode HCLK = 12 MHz while(1){} Executed from Flash	-	2.8	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	12 MHz	X	V
I_{DD10}		-	2.3	-	mA	5.5V	12 MHz	X	X
I_{DD11}		-	2.8	-	mA	3V	12 MHz	X	V
I_{DD12}		-	2.3	-	mA	3V	12 MHz	X	X

I_{DD13}	Operating Current Normal Run Mode HCLK = 4 MHz while(1){} Executed from Flash	-	1.2	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	4 MHz	X	V
I_{DD14}		-	1.0	-	mA	5.5V	4 MHz	X	X
I_{DD15}		-	1.2	-	mA	3V	4 MHz	X	V
I_{DD16}		-	1.0	-	mA	3V	4 MHz	X	X
I_{DD17}	Operating Current Normal Run Mode HCLK = 32 kHz while(1){} Executed from Flash	-	291.7	-	µA	V_{DD}	LXT	LIRC	All Digital Modules
						5.5V	32 KHz	V	V[1]
I_{DD18}		-	290.7	-	µA	5.5V	32 KHz	V	X
I_{DD19}		-	280.8	-	µA	3V	32 KHz	V	V[1]
I_{DD20}		-	281.4	-	µA	3V	32 KHz	V	X
I_{DD17}	Operating Current Normal Run Mode HCLK = 10 kHz while(1){} Executed from Flash	-	248.0	-	µA	V_{DD}	HXT	LIRC	All Digital Modules
						5.5V	X	10 KHz	V[2]
I_{DD18}		-	247.7	-	µA	5.5V	X	10 KHz	X
I_{DD19}		-	237.9	-	µA	3V	X	10 KHz	V[2]
I_{DD20}		-	237.5	-	µA	3V	X	10 KHz	X
I_{IDLE5}	Operating Current Idle Mode HCLK= 48 MHz	-	4.9	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	X	V	V
I_{IDLE6}		-	2.6	-	mA	5.5V	X	V	X
I_{IDLE7}		-	4.9	-	mA	3V	X	V	V
I_{IDLE8}		-	2.6	-	mA	3V	X	V	X
I_{IDLE1}	Operating Current Idle Mode HCLK = 24 MHz	-	2.8	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	24 MHz	X	V
I_{IDLE2}		-	1.9	-	mA	5.5V	24 MHz	X	X
I_{IDLE3}		-	2.8	-	mA	3V	24 MHz	X	V
I_{IDLE4}		-	1.9	-	mA	3V	24 MHz	X	X
I_{IDLE9}	Operating Current Idle Mode	-	2.0	-	mA	V_{DD}	HXT	HIRC	All Digital Modules

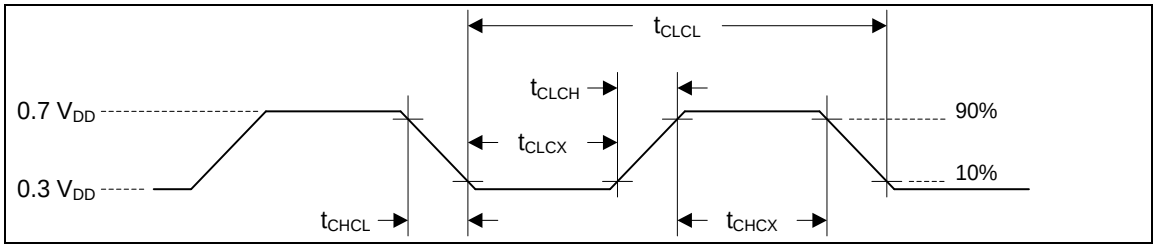
	HCLK = 16 MHz					5.5V	V	X	V
I_{IDLE10}		-	1.3	-	mA	5.5V	V	X	X
I_{IDLE11}		-	2.0	-	mA	3V	V	X	V
I_{IDLE12}		-	1.4	-	mA	3V	V	X	X
I_{IDLE9}	Operating Current Idle Mode HCLK = 12 MHz	-	1.5	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE10}		-	1.0	-	mA	5.5V	V	X	X
I_{IDLE11}		-	1.5	-	mA	3V	V	X	V
I_{IDLE12}		-	1.0	-	mA	3V	V	X	X
I_{IDLE13}	Operating Current Idle Mode HCLK = 4 MHz	-	0.8	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE14}		-	0.6	-	mA	5.5V	V	X	X
I_{IDLE15}		-	0.7	-	mA	3V	V	X	V
I_{IDLE16}		-	0.6	-	mA	3V	V	X	X
I_{DD17}	Operating Current Idle Mode HCLK = 32 kHz	-	274.3	-	µA	V_{DD}	HXT	LIRC	All Digital Modules
						5.5V	X	V	V[1]
I_{DD18}		-	273.0	-	µA	5.5V	X	V	X
I_{DD19}		-	265.0	-	µA	3V	X	V	V[1]
I_{DD20}		-	263.9	-	µA	3V	X	V	X
I_{DD17}	Operating Current Idle Mode HCLK = 10 kHz	-	232.6	-	µA	V_{DD}	HXT	LIRC	All Digital Modules
						5.5V	X	V	V[2]
I_{DD18}		-	232.2	-	µA	5.5V	X	V	X
I_{DD19}		-	222.5	-	µA	3V	X	V	V[2]
I_{DD20}		-	222.1	-	µA	3V	X	V	X
I_{PWD1}	Standby Current Power-down Mode (Deep Sleep Mode)	-	3.7	-	µA	V_{DD} = 5.5 V, All oscillators and analog blocks turned off.			
I_{PWD2}		-	2.5	-	µA	V_{DD} = 3 V, All oscillators and analog blocks turned off.			
I_{LK}	Input Leakage Current PA/PB/PC/PD	-1	-	+1	µA	V_{DD} = 5.5 V, 0 < V_{IN}< V_{DD} Open-drain or input only mode			

V_{IL1}	Input Low Voltage PA/PB/PC/PD (TTL Input)	-0.3	1.33		V	V_{DD} = 5.5 V
		-0.3	1			V_{DD} = 3.3 V
V_{IH1}	Input High Voltage PA/PB/PC/PD (TTL Input)		1.47	V_{DD} + 0.3	V	V_{DD} = 5.5 V
			1.08	V_{DD} + 0.3		V_{DD} = 3.3 V
V_{ILS}	Negative-going Threshold (Schmitt Input), nRESET	-	-	$0.3V_{DD}$	V	-
V_{IHS}	Positive-going Threshold (Schmitt Input), nRESET	$0.7V_{DD}$	-	-	V	-
R_{UP}[3]	Internal Pull-up Resistor (PA/PB/PC/PD)		86		kΩ	V_{DD} = 3.3V
			51		kΩ	V_{DD} = 5.5V
R_{LOW}[3]	Internal Pull-low Resistor (PA/PB/PC/PD)		97		kΩ	V_{DD} = 3.3V
			56		kΩ	V_{DD} = 5.5V
R_{RST}[3]	Internal nRESET Pin Pull-up Resistor	48		148	kΩ	V_{DD} = 2.1 V ~ 5.5V
V_{ILS}	Negative-going Threshold (Schmitt input), PA/PB/PC/PD	-	-	$0.3V_{DD}$	V	-
V_{IHS}	Positive-going Threshold (Schmitt input), PA/PB/PC/PD	$0.7V_{DD}$	-	-	V	-
I_{IL}	Logic 0 Input Current PA/PB/PC/PD (Quasi-bidirectional Mode)	-	-63.65		μA	V_{DD} = 5.5 V, V_{IN} = 0V
I_{TL}	Logic 1 to 0 Transition Current PA/PB/PC/PD	-	-566.7	-	μA	V_{DD} = 5.5 V
I_{SR11}	Source Current PA/PB/PC/PD (Quasi-bidirectional Mode)	-	-372	-	μA	V_{DD} = 4.5 V, V_{IN} = 2.4 V
I_{SR12}		-	-76.8	-	μA	V_{DD} = 2.7 V, V_{IN} = 2.2 V
I_{SR13}		-	-37.3	-	μA	V_{DD} = 2.1 V, V_{IN} = 1.8 V
I_{SR21}	Source Current PA/PB/PC/PD (Push-pull Mode)	-	-19.2	-	mA	V_{DD} = 4.5 V, V_{IN} = 2.4 V
I_{SR22}		-	-4	-	mA	V_{DD} = 2.7 V, V_{IN} = 2.2 V
I_{SR23}		-	-2	-	mA	V_{DD} = 2.1 V, V_{IN} = 1.8 V
I_{SK11}	Sink Current PA/PB/PC/PD (Quasi-bidirectional, Open-Drain and Push-pull Mode)	-	12.8	-	mA	V_{DD} = 4.5 V, V_{IN} = 0.4 V
I_{SK12}		-	8.1	-	mA	V_{DD} = 2.7 V, V_{IN} = 0.4 V
I_{SK13}		-	6	-	mA	V_{DD} = 2.1 V, V_{IN} = 0.4 V

Notes:
1. Only enable modules which support 32 kHz LIRC clock source
2. Only enable modules which support 10 kHz LIRC clock source
3. Guaranteed by design, not test in production.

7.3 AC Electrical Characteristics

7.3.1 External Input Clock



Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

7.3.2 External 4~24 MHz High Speed Crystal (HXT)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{HXT}	Operation Voltage	2.1	-	5.5	V	-
T_A	Temperature	-40	-	105	℃	-
I_{HXT}	Operating Current	-	414	-	uA	12 MHz, V_{DD} = 5.5V
f_{HXT}	Clock Frequency	4	-	24	MHz	-

7.3.3 Typical Crystal Application Circuits

Crystal	C1	C2
4 MHz ~ 24 MHz	10~20 pF	10~20 pF

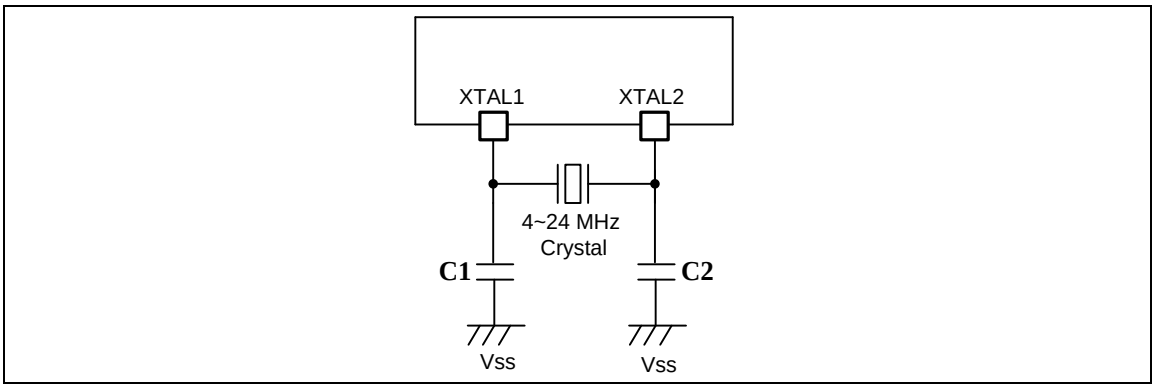


Figure 7-1 NM1120 Typical Crystal Application Circuit

7.3.4 48 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	-	1.5	-	V	-
f_{HRC}	Center Frequency	-	48	-	MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	T_A = 25 ℃ V_{DD} = 5.5 V
		-2%	-	2%	%	T_A = -40℃~105℃ V_{DD}=2.5 V~ 5.5 V
I_{HRC}	Operating Current	-	1090	-	μA	T_A = 25 ℃,V_{DD} = 5 V

7.3.5 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{LRC}	Supply Voltage	-	1.5V	-	V	-
f_{LRC}	Center Frequency	-	10	-	kHz	-
	Oscillator Frequency	-50[1]	-	+50[1]	%	V_{DD} = 2.1 V ~ 5.5 V T_A = -40℃ ~ +105℃
I_{LRC}	Operating Current	-	0.4	-	μA	T_A = 25 ℃,V_{DD} = 5 V

Note1: These parameters are characterized but not tested.

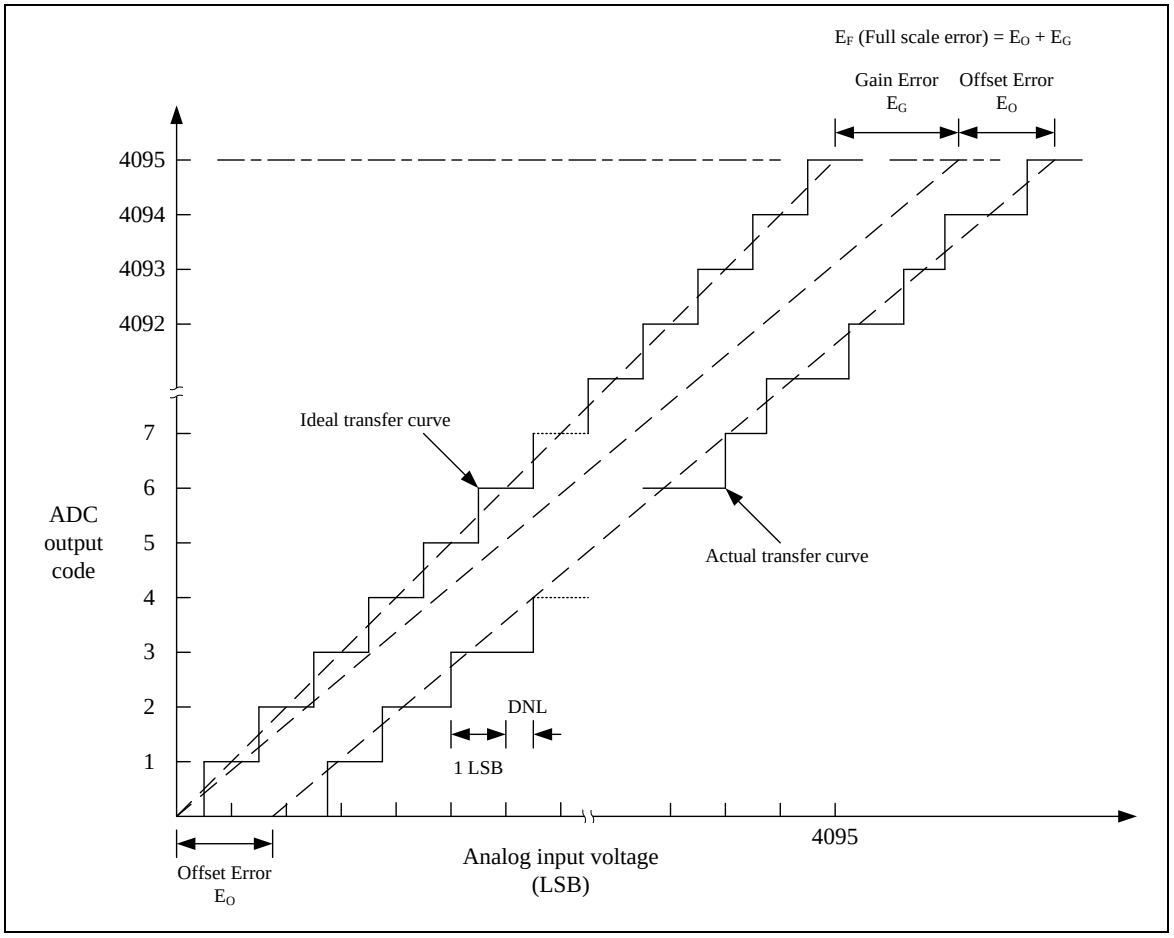
7.4 Analog Characteristics

7.4.1 12-bit SAR ADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	12	Bit	-
DNL	Differential Nonlinearity Error	-	2	-	LSB	V_{DD} = 3.0 ~5.5 V
INL	Integral Nonlinearity Error	-	±2	-	LSB	V_{DD} = 3.0 ~5.5 V
E_O	Offset Error	-	±1	-	LSB	V_{DD} = 3.0 ~5.5 V
E_G	Gain Error (Transfer Gain)	-	-1	-	LSB	V_{DD} = 3.0 ~5.5 V
E_A	Absolute Error	-	±3	-	LSB	V_{DD} = 3.0 ~5.5 V
-	Monotonic	Guaranteed			-	-
F_{ADC}	ADC Clock Frequency		12	16	MHz	V_{DD} = 3.0 ~5.5 V
T_{ACQ}	Acquisition Time (Sample Stage)	N+1			$1/F_{ADC}$	V_{DD} = 3.0 ~5.5 V N is sampling counter, N=1~1024
		200			ns	V_{DD} = 3.0~5.5 V
T_{CONV}	Conversion Time[3]	-	1000	1500	ns	V_{DD} = 3.0~5.5 V
V_{DD}	Supply Voltage	3.0	-	5.5	V	-
I_{DDA}	Supply Current (Avg.)	-	1	-	mA	V_{DD} = 5.5 V
V_{IN}	Analog Input Voltage	0	-	AV_{DD}	V	-
C_{IN}	Input Capacitance[2]	-	1.6	-	pF	-
R_{IN}	Input Load[2]	-	2.5	-	kΩ	-

Note:

1. ADC voltage reference is same with V_{DD} .
2. It's for sample and hold. The maximum value depends on process variation. Basically, the variation of CIN is less than about 10% of typical value and the variation of RIN is less about 20% of typical value.
3. Guaranteed by design, not test in production. The conversion time is upto auto-completion of analog comparison in ADC IP and the typical value is about 1000ns at V_{DD} = 5V.



7.4.2 LDO & Power Management

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	DC Power Supply	2.1	-	5.5	V	-
V_{LDO}	Output Voltage		1.5		V	-
T_A	Temperature	-40	25	105	℃	

Notes:
It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

7.4.3 Low Voltage Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	2.1	-	5.5	V	-
V_{LVR}	Threshold Voltage(high→low)	1.8	1.9	2.0	V	T_A = -40℃ ~ +105℃
V_{LVRHYS}	Hysteresis Voltage	-	-	100	mV	T_A = -40℃ ~ +105℃

7.4.4 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-
T_A	Temperature	-40	25	105	℃	-
I_{BOD}	Quiescent Current	-	100	-	μA	AV_{DD} =5.5V
V_{BOD}	Brown-out Detector	4.2	4.3	4.4	V	BOV_VL [2:0] = 7
		3.9	4.0	4.1	V	BOV_VL [2:0] = 6
		3.6	3.7	3.8	V	BOV_VL [2:0] = 5
		2.9	3.0	3.1	V	BOV_VL [2:0] = 4
		2.6	2.7	2.8	V	BOV_VL [2:0] = 3
		2.3	2.4	2.5	V	BOV_VL [2:0] = 2
		2.1	2.2	2.3	V	BOV_VL [2:0] = 1
		1.9	2.0	2.1	V	BOV_VL [2:0] = 0

7.4.5 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	105	℃	-
V_{POR}	Threshold Voltage		1.75		V	V_{DD}=5.0V
V_{POR-ST}	V_{DD} start voltage to ensure Power-on Reset			100	mV	
RR_{VDD}	V_{DD} Raising Rate to ensure Power-on Reset	0.125		25	V/ms	0-2.5V in 20ms
t_{POR}	Minimum time for V_{DD} stays at V_{POR} to ensure Power-on Reset	0.5			ms	

Note: Guaranteed by design, not test in production

7.4.6 Comparator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{CMP}	Supply Voltage	2.1	-	5.5	V	
T_A	Temperature	-40	25	105	℃	-
I_{CMP}	Operation Current	-	47		μA	V_{DD}=5.5V
V_{OFF}	Input Offset Voltage		±10		mV	-
V_{SW}	Output Swing	0	-	V_{DD}	V	-
V_{COM}	Input Common Mode Range	0.1	-	AV_{DD} – 0.1	V	-
-	DC Gain[1]	-	60	-	dB	-
T_{PGD}	Propagation Delay	-	225	-	ns	
V_{HYS}	Hysteresis	-	10	-	mV	ACMPPHYSEN = 01
V_{HYS}	Hysteresis	-	90	-	mV	ACMPPHYSEN = 10
T_{STB}	Stable time	-	1.06	-	μs	

Notes:
Guaranteed by design, not test in production.

7.4.7 PGA

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
	Operation voltage range	2.5	3.3	5.5	V	
	Operating Current			5	mA	V_{DD}=5V, T=125℃
	Operating Temperature	-40	25	125	℃	
	Input Offset Voltage	-9.5	-3	9.5	mV	T_A= -40~105℃ ,V_{DD}=5V V_{CM}=V_{DD}/2, Gain=2
	Output Swing	0.1		V_{DD} - 0.1	V	
	PGA gain accuracy	-1		+1	%	
	Input Common Mode Range	0		V_{DD} - 1.5	V	
	DC Gain	50	80		dB	
	Unity Gain Frequency	7		8.2	MHz	V_{DD}=5V
	Phase Margin	50°			°	
	PSRR+	49	90		dB	V_{DD}=5V
	CMRR	69	90		dB	V_{DD}=5V
	Slew Rate+		6.0	7.5	V/us	V_{DD}=5V, RLoad=1.3K, CLoad=100p
	Wake Up Time			20	us	
	Maximum output voltage swing from rail		40		mV	V_{DD}=5.5V, RL=50K
			200		mV	V_{DD}=5.5V, RL=10K

Notes:
Guaranteed by design, not test in production.

7.4.8 Temperature Sensor

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
TA	Temperature	-40	-	105	℃	
-	Gain [1,]	-	-1.81	-	mV/℃	
-	Offset [1,2]	-	725	-	mV	TA = 0 ℃

Note:
1. The temperature sensor formula for the output voltage (Vtemp) is list as below equation.
   Vtemp (mV) = Gain (mV/℃) x Temperature (℃) + Offset (mV)
2. The Gain and Offset may have some drift for different chips. Register SYS_TSOFFSET is a reference data measured by ADC in factory test.

7.4.9 ESD Characteristics

Symbol	Ratings	Condition	Package	Maximum Value	Unit
V_{ESD}	Electrostatic discharge (Human body mode)	TA = + 25 ℃	TSSOP 20 TSSOP 28 QFN20	7000	V
	Electrostatic discharge (Machine mode)			300	V
	Electrostatic discharge (Charged Device mode)			750	V

7.4.10 EFT Characteristics

Symbol	Condition	Package	Pass level	Unit
	Fsys			
	HIRC	TSSOP 20 TSSOP 28 QFN 20	± 4400	V

7.5 Flash DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[2]	Supply Voltage	1.35	1.5	1.65	V	
N_{ENDUR}	Endurance	20,000	-	-	cycles[1]	
T_{RET}	Data Retention	10	-	-	year	T_A =85℃
T_{ERASE}	Sector Erase Time	-		5	ms	
T_{PROG}	Program Time	-	7.5	-	us	
I_{DD1}	Read Current	-	3	4.5	mA	@33MHz
I_{DD2}	Program Current	-		4	mA	
I_{DD3}	Erase Current	-	2	-	mA	

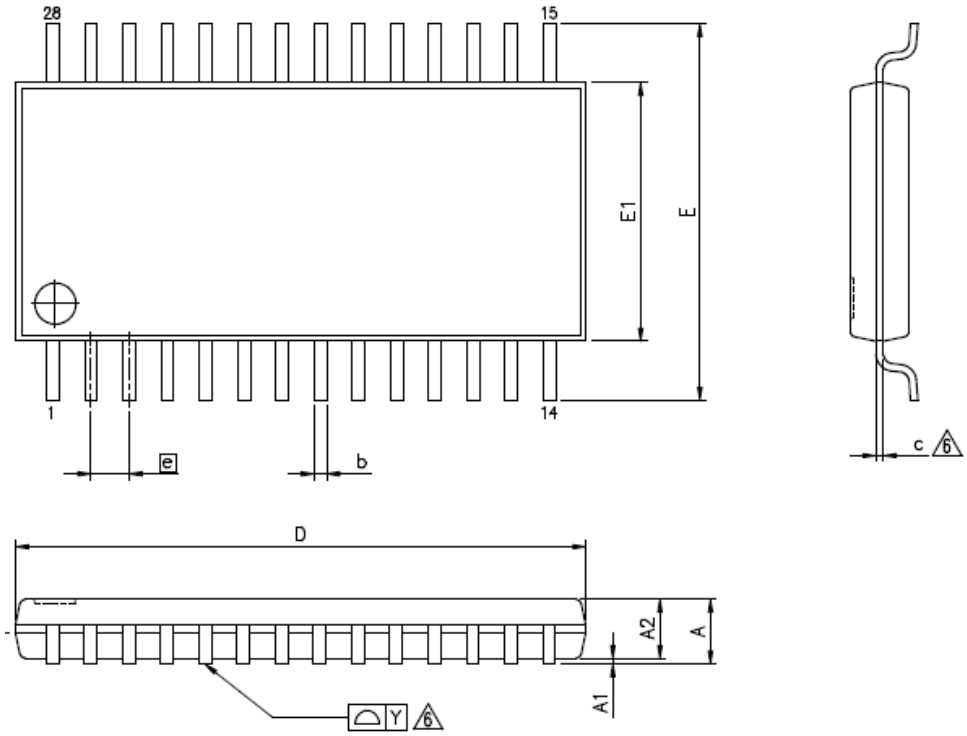
Notes:

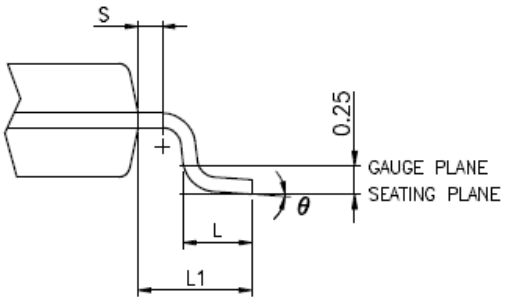
1. Number of program/erase cycles.
2. V_{FLA} is source from chip LDO output voltage.
3. Guaranteed by design, not test in production.

8 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

8.1 28-Pin TSSOP

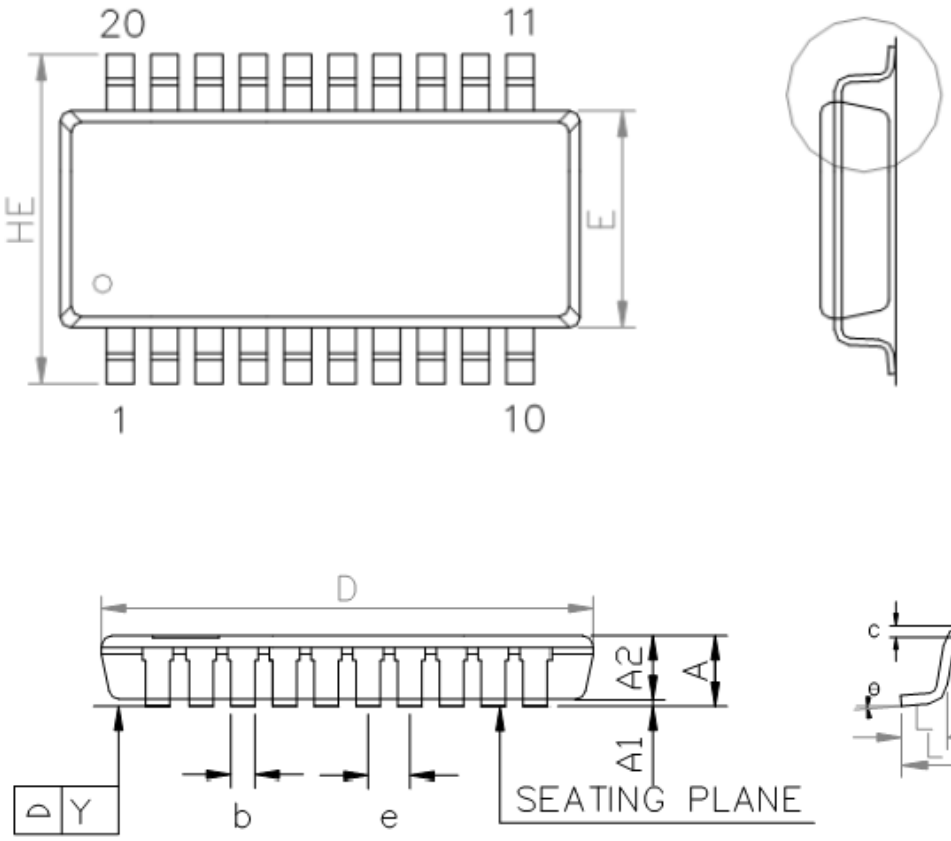




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

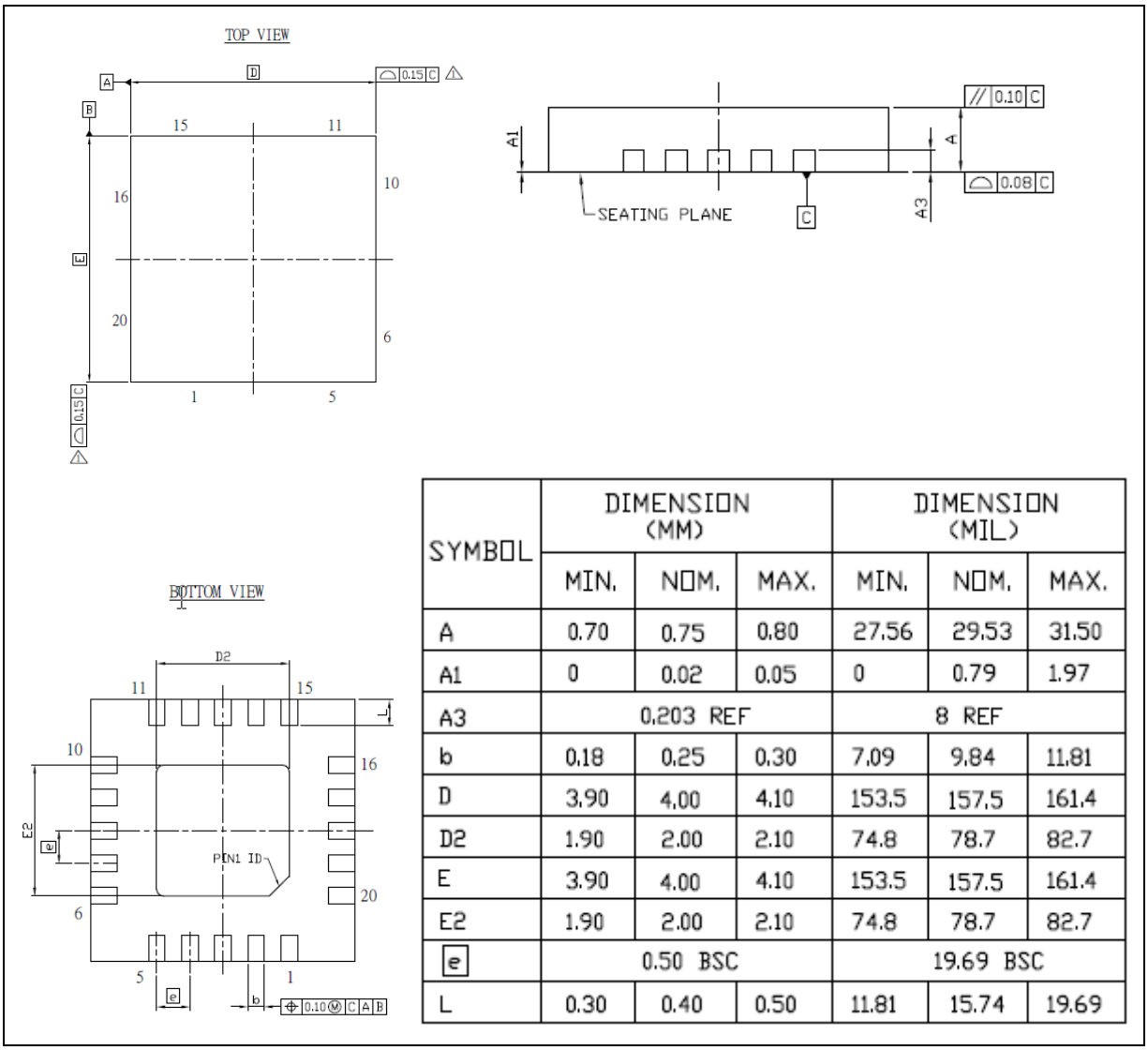
SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°
Y	0.10		

8.2 20-Pin TSSOP



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	-	0.30	0.007	-	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	-	0.20	0.004	-	0.008
θ	0°	-	8°	0°	-	8°
Y	0.10 BASIC			0.004 BASIC		

8.3 20-Pin QFN20 (4 mm x 4 mm)



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.56	29.53	31.50
A1	0	0.02	0.05	0	0.79	1.97
A3		0.203 REF			8 REF	
b	0.18	0.25	0.30	7.09	9.84	11.81
D	3.90	4.00	4.10	153.5	157.5	161.4
D2	1.90	2.00	2.10	74.8	78.7	82.7
E	3.90	4.00	4.10	153.5	157.5	161.4
E2	1.90	2.00	2.10	74.8	78.7	82.7
e		0.50 BSC			19.69 BSC	
L	0.30	0.40	0.50	11.81	15.74	19.69

9 REVISION HISTORY

Date	Revision	Description
2020.04.30	1.12	Preliminary version sychronized with TRM V1.12
2021.01.05	1.20	Modify the content of section 7.4.3 Low Voltage Reset
2022.06.23	1.21	Modify some typo.
2022.11.08	1.22	Add “Package is Halogen-free, RoHS-compliant and TSCA-compliant.” In chapter 2 and 8.
2023.11.02	1.23	Add circuit design note for nRESET pin.
2024.05.29	1.24	Add Power-on Reset on 7.4.5 page 83.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, “Insecure Usage”.

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer’s risk, and in the event that third parties lay claims to Nuvoton as a result of customer’s Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

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