MCX A175/176/185/186/255/256/265/266

Enhanced Arm Cortex-M33 MCU with 180/240 MHz, up to 1024 KB Flash, and Security

Rev. 5 — 6 July 2026 Product data sheet

- This document provides electrical specifications for MCX A175/176/185/186/255/256/265/266 family.
- For functional characteristics and the programming model, see MCX A175/176/185/186/255/256/265/266 Reference Manual.

1 Introduction

Features

- Arm® Cortex®-M33 180MHz with 738 CoreMark® (4.10 CoreMark®/MHz) for MCXA175/176/255/256
- Arm Cortex-M33 240 MHz with 984 CoreMark (4.10 CoreMark/MHz) for MCXA185/186/265/266
- Up to 1 MB Flash, 256 KB SRAM, up to 8 KB RAM with ECC
- All RAM can be retained down to Deep Power Down mode
- Internal free running oscillator (FRO180M) with ±1% precision across the full temperature range
- Temperature range: -40 °C to 125 °C
- Down to 78 µA/MHz Active current, 96 µA Deep Sleep current, 32 µA Power Down current, 473 nA Deep Power Down current

Cores

- Arm 32-bit Cortex-M33 CPU, with FPU and DSP extension instruction set and MPU, no Trust Zone

Processing Accelerators

- SmartDMA, co-processor for applications such as parallel camera interface and keypad scanning

Memories

- Single-bank Flash: Up to 1024 KB Flash with ECC (support one bit correction and two bits detection)
- Cache Engine with 8 KB RAM
- Up to 256 KB RAM of which 8 KB is shared with cache, configurable as up to 8 KB RAM with ECC (support one bit correction and two bits detection)
- All RAM can be retained down to Deep Power Down mode
- ROM

Security

- EdgeLock Accelerator
  - TRNG
  - PKC (Public Key Cryptography), supports ECC and RSA encryption and decryption
  - SGI (Secure Generic Interface), provides AES256, SHA-2 and key generation/derivation
  - Secure key store with key usage policies (protection of platform integrity, manufacturing and applications keys)
- 128-bit Universal Unique Identifier (UUID) per device in accordance with IETF's RFC4122 version5 specification
- Device lifecycle management
- Flash read/write/execute permission protect by MBC and lockable
- Implicit-protected Flash Region (IFR)
- Security Monitoring:
  - Code Watchdog for code flow integrity checking
  - 6x Passive anti tamper pin detect
  - GLIKEY enforces security checks before allowing a write to security-sensitive register
- Secure Installer for secure manufacturing and IP theft protection in untrusted factory

Low-Power Performance

- **Active**

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  - 78 µA/MHz, in Active Mode (executing while(1) from flash, 3.3 V at 25 °C)
- **Deep Sleep**
  - 96 µA, 9.01 µs wake-up (3.3 V at 25 °C)
- **Power Down**
  - 32 µA, 18.84 µs wake-up (full SRAM retention, 3.3 V at 25 °C)
- **Deep Power Down**
  - 473 nA, 1.57 ms wake-up (wakeup timer disabled, reset pin enabled, all SRAM off, 3.3 V at 25 °C)

System and Clocks

- 180 MHz free-running oscillator (FRO180M)
  - Can be configured to 240MHz via software, applicable only to MCXA18x and MCXA26x devices
- 12 MHz free-running oscillator (FRO12M)
- 16 kHz free-running oscillator (FRO16K)
- Up to 50 MHz crystal oscillator
- One PLL
- Hardware and Software Watchdogs
- Asynchronous DMA modules (8-channels)

Communication Interfaces for Connectivity

- 2x LPSPI, 4x LPI2C, 6x LPUART
  - MCXA175/176/255/256 support 5x LPUART
- 1x I3C
- USB Full-speed (Device/Host) with on-chip FS PHY
- Up to 2x FlexCAN with FD
- FlexIO

Human Machine Interface

- 4 x 44 segment LCD interface

Advanced Motor Control

- Up to 2x FlexPWM, each FlexPWM has 4 sub-modules, providing 16 complementary outputs for each (no Nanoedge module)
- Up to 2x Quadrature Encoder/Decoder (eQDC)
- 2x AOI (AND/OR/Invert) modules support up to 4 output triggers

Analog

- 2x 16-bit ADC
  - Up to 3.2 Msps in 16-bit mode, and 4 Msps in 12-bit mode
  - Up to 43 ADC Input channels total (depending on the package)
  - Integrated temperature sensor
- 1 x 12-bit DAC
  - Up to 1 Msps
- 2 x High-speed Comparators with 8 input pins and 8-bit DAC as internal reference

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  - 1x LPCMP is functional down to Deep Power Down mode
- 1x OPAMP without PGA

Timers

- 5x 32-bit standard general-purpose asynchronous timers/counters (CTimer), each CTimer supports up to 4x capture inputs and 4x compare outputs, 3x PWM outputs. Specific timer events can be selected to generate DMA requests.
- Low power timer
- Frequency measurement timer
- Windowed watchdog timer
- Wake timer
- Micro-tick timer (UTICK)
- OS event timer
- RTC timer without external 32KHz input

General-purpose input/outputs

- Up to 114 GPIOs
- Up to eight 20 mA IO
- 50 MHz IO on P1, P3 and P4
- Up to 29-pin wake-up sources function down to deep power-down mode
- Support 1.71 V~3.6 V IO supply range

Power Management

- Integrated voltage regulator
  - Core LDO, other LDOs
- Operating voltage: 1.71 V to 3.6 V
- I/Os: 1.71 V - 3.6 V full-performance

Target Applications

Industrial

- Energy Storage and Management System
- Smart Metering
- Factory Automation
- Industrial HMI
- Mobile Robotics Ecosystem
- Motion Control and Robotics
- Motor Drives
- Brushless DC Motor (BLDC) Control
- Permanent Magnet Synchronous Motor (PMSM) Control

Smart Home

- Home Control Panel
- Major Home Appliances
- Robotic Appliance

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- Smart Speaker
- Soundbar
- Gaming Accessories
- Smart Lighting
- Smart Power Socket and Light Switch

Table 1. Ordering Information

Part Number [1][2]	Marking	Core Speed (MHz)	Flash (KB)	SRAM (KB)	GPIO	Pin Count	Package
MCXA175VPN	MA175N	180	512	128	114	169	WFBGA
MCXA175VLQ	MCXA175VLQ	180	512	128	114	144	LQFP
MCXA175VLL	MCXA175VLL	180	512	128	83	100	LQFP
MCXA175VLH	MCXA175VLH	180	512	128	52	64	LQFP
MCXA176VPN	MA176N	180	1024	256	114	169	WFBGA
MCXA176VLQ	MCXA176VLQ	180	1024	256	114	144	LQFP
MCXA176VLL	MCXA176VLL	180	1024	256	83	100	LQFP
MCXA176VLH	MCXA176VLH	180	1024	256	52	64	LQFP
MCXA185VPN	MA185N	240	512	128	114	169	WFBGA
MCXA185VLQ	MCXA185VLQ	240	512	128	114	144	LQFP
MCXA185VLL	MCXA185VLL	240	512	128	83	100	LQFP
MCXA185VLH	MCXA185VLH	240	512	128	52	64	LQFP
MCXA186VPN	MA186N	240	1024	256	114	169	WFBGA
MCXA186VLQ	MCXA186VLQ	240	1024	256	114	144	LQFP
MCXA186VLL	MCXA186VLL	240	1024	256	83	100	LQFP
MCXA186VLH	MCXA186VLH	240	1024	256	52	64	LQFP
MCXA255VPN	MA255N	180	512	128	114	169	WFBGA
MCXA255VLQ	MCXA255VLQ	180	512	128	114	144	LQFP
MCXA255VLL	MCXA255VLL	180	512	128	83	100	LQFP
MCXA255VLH	MCXA255VLH	180	512	128	52	64	LQFP
MCXA256VPN	MA256N	180	1024	256	114	169	WFBGA
MCXA256VLQ	MCXA256VLQ	180	1024	256	114	144	LQFP
MCXA256VLL	MCXA256VLL	180	1024	256	83	100	LQFP
MCXA256VLH	MCXA256VLH	180	1024	256	52	64	LQFP
MCXA265VPN	MA265N	240	512	128	114	169	WFBGA
MCXA265VLQ	MCXA265VLQ	240	512	128	114	144	LQFP
MCXA265VLL	MCXA265VLL	240	512	128	83	100	LQFP

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Table 1. Ordering Information *...continued*

Part Number [1][2]	Marking	Core Speed (MHz)	Flash (KB)	SRAM (KB)	GPIO	Pin Count	Package
MCXA265VLH	MCXA265VLH	240	512	128	52	64	LQFP
MCXA266VPN	MA266N	240	1024	256	114	169	WFBGA
MCXA266VLQ	MCXA266VLQ	240	1024	256	114	144	LQFP
MCXA266VLL	MCXA266VLL	240	1024	256	83	100	LQFP
MCXA266VLH	MCXA266VLH	240	1024	256	52	64	LQFP

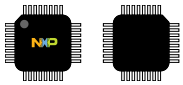
[1] As marked on package
[2] To confirm current availability of orderable part numbers, go to http://www.nxp.com and perform a part number search.

Table 2. Device isometric diagram



BGA169

7 x 7 x 0.8 mm, 0.5 mm



LQFP144

20 x 20 x 1.4 mm, 0.5 mm

LQFP100

14 x 14 x 1.4 mm, 0.5 mm

LQFP64

10 x 10 x 1.4 mm, 0.5 mm

Table 3. Device Revision Number

Device Mask Set Number	JTAG ID Register[PRN]
0P89K	0x0726802B

Table 4. Related Resources

Type	Description	Resource
Fact Sheet	The Fact Sheet gives overview of the product key features and its uses.	MCXA1xx_FS and MCXA2xx_FS
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	MCXAP144M240F61RM
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	MCXAP144M240F61DS
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	MCXA266VLQ_0P89K
Package drawing	Package dimensions are provided in package drawings.	• WFBGA169: 98ASA02230D • LQFP144:98ASS23177W • LQFP100:98ASS23308W

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Table 4. Related Resources *...continued*

Type	Description	Resource
		• LQFP64:98ASS23234W
Software development kit	MCUXpresso SDK. An open source software development kit (SDK) built specifically for your processor and evaluation board selections.	http://www.nxp.com/mcuxpresso

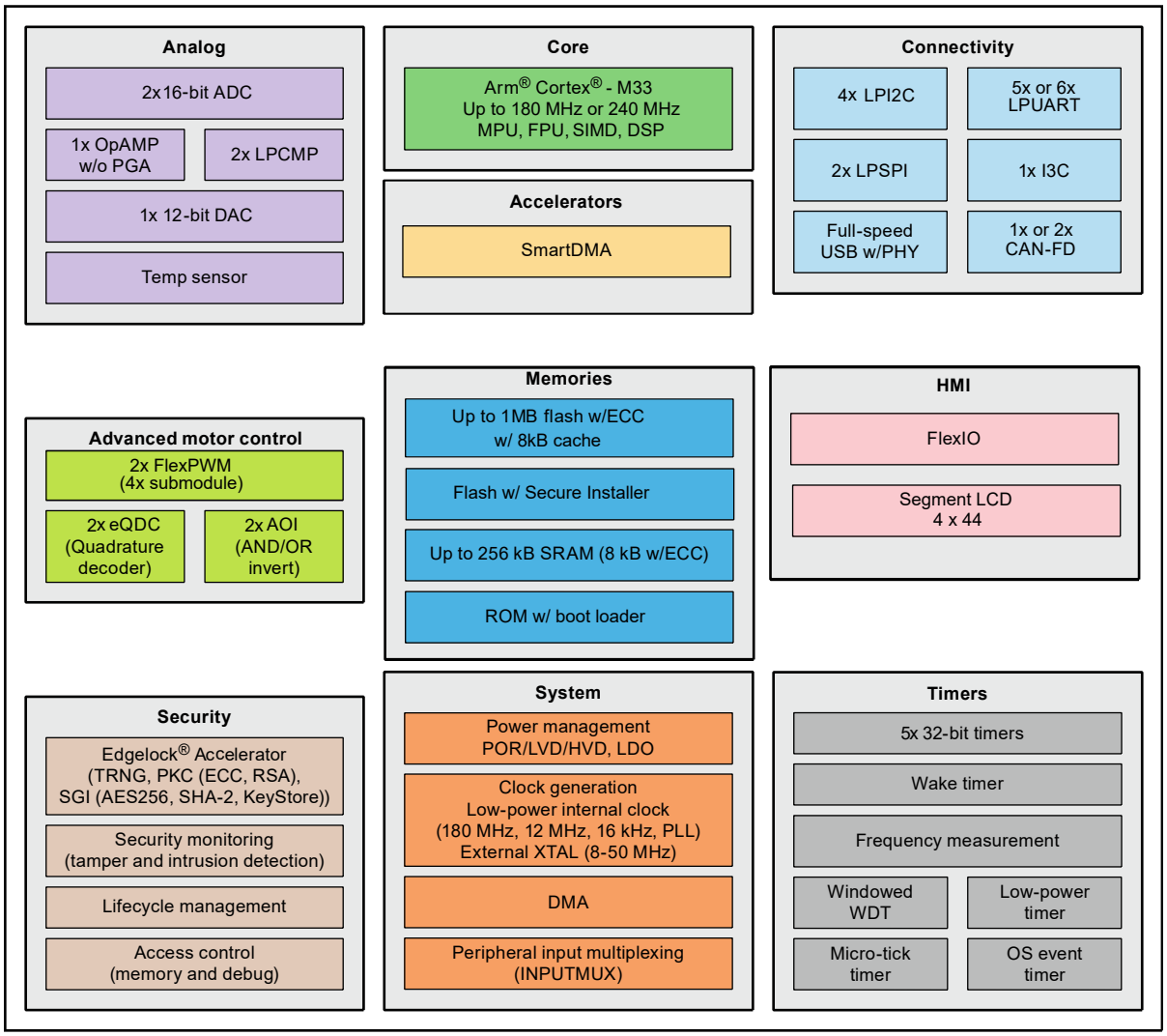


Figure 1. Block Diagram

Note: *Secure Installer is protected by ROM from read, write and execute.*

Note: *Secure Installer cannot be reprogrammed and no secure binary file (SB3.1) will be supported after SI is erased.*

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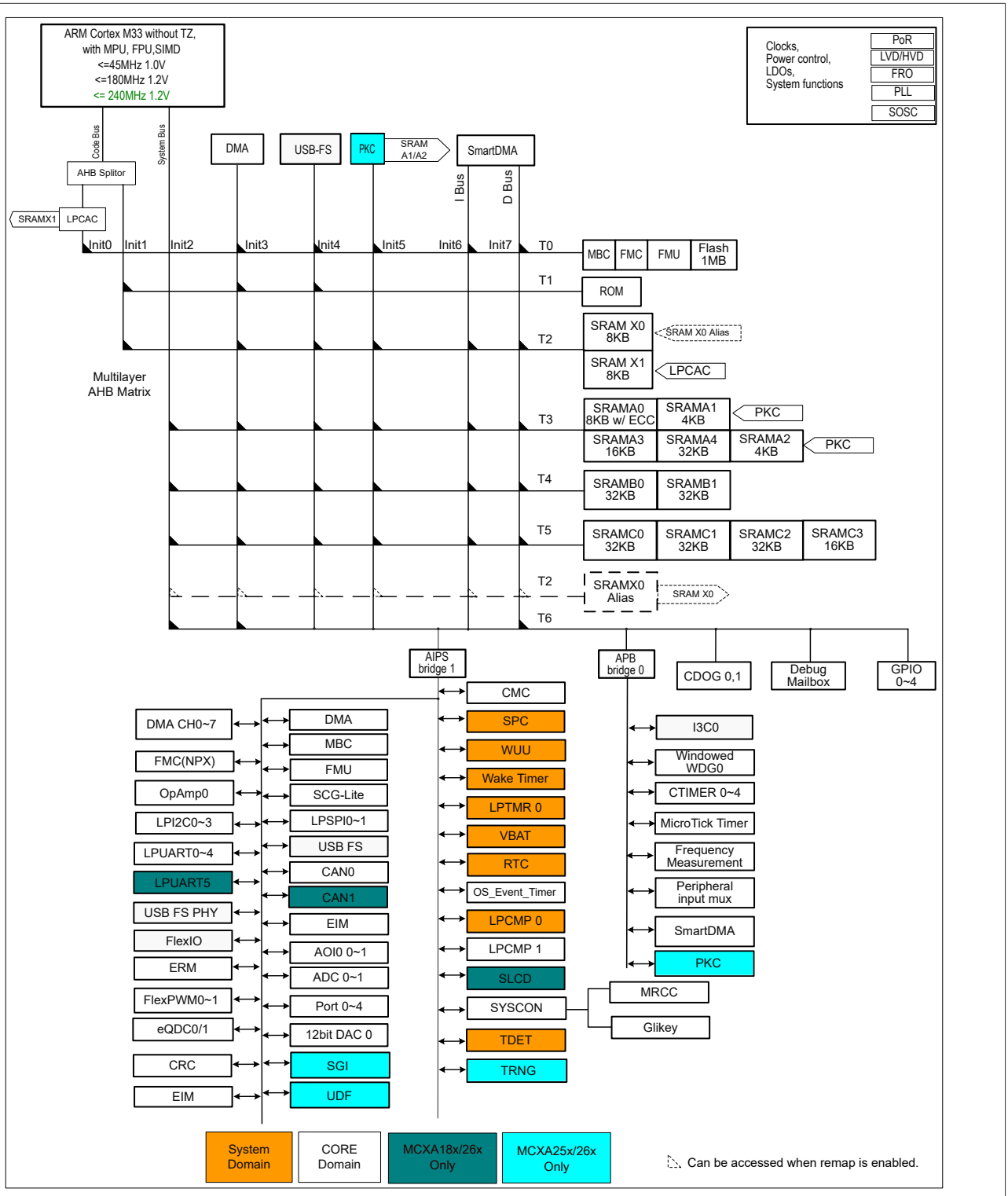


Figure 2. Bus Architecture

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2 Feature Comparison

Table 5. Feature Comparison

		MCX A175	MCX A176	MCX A255	MCX A256	MCX A185	MCX A186	MCX A265	MCX A266
Core Platform	Core Cortex-M33	180 MHz				240 MHz			
	Cache	8 KB							
	DMA	8 Channels							
	Wakeup unit(WUU)	Yes							
	Peripheral input multiplexing(INPUTMUX)	Yes							
Processing Accelerators	MAU	No							
	SmartDMA	Yes							
Clock	Fast internal reference clock FRO180M	180 MHz				180 MHz (or configure to 240 MHz)			
	Slow internal reference clock FRO12M	12 MHz							
	Low power internal reference clock FRO16K	16.384 kHz							
	System oscillator with external crystal(SOSC)	8 - 50 MHz							
	PLL	Yes							
Memory	Flash 512 KB version include 8 KB CMPA 1024 KB version include 8 KB CMPA MCXA25x/26x include 56 KB for Secure Installer	512 KB	1024 KB	512 KB	1024 KB	512 KB	1024 KB	512 KB	1024 KB
	SRAM 128 KB version include 8 KB with ECC 256 KB version include 8 KB with ECC and include 8 KB SRAM shared with Cache	128 KB	256 KB	128 KB	256 KB	128 KB	256 KB	128 KB	256 KB
	Error injection module (EIM)	Yes							
	Error recording module (ERM)	Yes							
Security	Lifecycle management (LC)	Yes							
	Read out protection (ROP)	Yes							

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Table 5. Feature Comparison...*continued*

			MCX A175	MCX A176	MCX A255	MCX A256	MCX A185	MCX A186	MCX A265	MCX A266
	Memory block checker (MBC)		Yes							
	GLIKEY		Yes							
	UUID		128-bit							
	Code watchdog (CDOG)		1		2		1		2	
	Cyclic redundancy check (CRC)		1							
	Secure key management		No		Yes		No		Yes	
	AES-256[1]		No		Yes		No		Yes	
	SHA2[1]		No		Yes		No		Yes	
	PKC[1]		No		Yes		No		Yes	
	TRNG[1]		No		Yes		No		Yes	
	AGDET[1]		No		Yes		No		Yes	
	Debug control[1]		No		Yes		No		Yes	
	Secure installer[1]		No		Yes		No		Yes	
	Passive anti tamper pin	WFBGA169(PN)	6							
		LQFP144(LQ)	6							
		LQFP100(LL)	4							
		LQFP64(LH)	2							
Communication Interfaces	LPUART		5				6			
	LPSPI		2							
	LPI2C		4							
	I3C		1							
	USB Full Speed Port (Host/ Device)		Device Only		Device/Host					
	FlexCAN		1x CAN FD				2x CAN FD			
	FlexIO		1							
HMI	Segmented LCD	WFBGA169(PN)	No				4 x 44			
		LQFP144(LQ)					4 x 44			
		LQFP100(LL)					4 x 36			
		LQFP64(LH)					4 x 22			
Analog	ADC		2							
	ADC Input Pins	WFBGA169(PN)	43							

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Table 5. Feature Comparison...*continued*

			MCX A175	MCX A176	MCX A255	MCX A256	MCX A185	MCX A186	MCX A265	MCX A266
		LQFP144(LQ)	43							
		LQFP100(LL)	39							
		LQFP64(LH)	28							
	Low power comparator(LPCMP)		2							
	DAC		1							
	OpAmp (w/o PGA)	WFBGA169(PN)	1							
		LQFP144(LQ)	1							
		LQFP100(LL)	1							
		LQFP64(LH)	1							
Motor Control	FlexPWM [2]		2							
	AND/OR INVERT (AOI)		2							
	Quadrature decoder (eQDC)		2							
Timer	32-bit timer(Ctimer)		5							
	Low power timer(LPTMR)		1							
	Micro-tick timer(UTICK)		1							
	OS event timer		1							
	Windowed watchdog timer (WWDT)		1							
	Frequency measurement (FREQME)		1							
	Wake timer		1							
	RTC[3]		1							
IO	Independent I/O supply[4]		No							
	5 V tolerant IO[5]		2							
	High drive IO (20 mA)[6]		Up to 8							
	50 MHz IO[7]		Up to 22							
Packages [8]	GPIO/ Wakeup Pin	WFBGA169(PN)	114/29							
		LQFP144(LQ)	114/29							
		LQFP100(LL)	83/25							
		LQFP64(LH)	52/19							
Temperature range			-40 ℃ to 125 ℃							

[1] This feature described in Security Reference Manuel (SRM), user can request SRM document from nxp.com under NDA.
[2] There are 4 sub-modules for each FlexPWM module.
[3] RTC only support counter mode, no dedicate VBAT and not support external 32.768 kHz crystal.
[4] Does not support 1.2 V I/O power supply.

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[5] P3_27, P3_28 are 5 V tolerant I/Os
[6] P1_8,P1_9,P1_30,P1_31,P3_1,P3_0,P0_16,P0_17 are High Drive I/Os
[7] 50 MHz I/Os are located on P1, P3, P4 ports
[8] Show the package types and GPIO numbers and Wakeup pin numbers

Table 6. SRAM and Flash address information

Memory			MCX A175 MCX A185	MCX A255 MCX A265	MCX A176 MCX A186	MCX A256 MCX A266
Code bus memory [1]						
Flash	User Flash	Start	0x00000000	0x00000000	0x00000000	0x00000000
		End	0x0007DFFF	0x0006FFFF	0x000FDFFF	0x000EFFFF
	Secure Installer	Start	—	0x00070000	—	0x000F0000
		End	—	0x0007DFFF	—	0x000FDFFF
	CMPA [2]	Start	0x0007E000	0x0007E000	0x000FE000	0x000FE000
		End	0x0007FFFF	0x0007FFFF	0x000FFFF	0x000FFFF
SRAM	SRAM X0	Start	0x04000000	0x04000000	0x04000000	0x04000000
		End	0x04001FFF	0x04001FFF	0x04001FFF	0x04001FFF
	SRAM X1	Start	0x04002000	0x04002000	0x04002000	0x04002000
		End	0x04003FFF	0x04003FFF	0x04003FFF	0x04003FFF
System bus RAM						
SRAM	SRAM A0	Start	0x20000000	0x20000000	0x20000000	0x20000000
		End	0x20001FFF	0x20001FFF	0x20001FFF	0x20001FFF
	SRAM A1	Start	0x20002000	0x20002000	0x20002000	0x20002000
		End	0x20002FFF	0x20002FFF	0x20002FFF	0x20002FFF
	SRAM A2	Start	0x20003000	0x20003000	0x20003000	0x20003000
		End	0x20003FFF	0x20003FFF	0x20003FFF	0x20003FFF
	SRAM A3	Start	0x20004000	0x20004000	0x20004000	0x20004000
		End	0x20007FFF	0x20007FFF	0x20007FFF	0x20007FFF
	SRAM A4	Start	0x20008000	0x20008000	0x20008000	0x20008000
		End	0x2000FFFF	0x2000FFFF	0x2000FFFF	0x2000FFFF
	SRAM B0	Start	0x20010000	0x20010000	0x20010000	0x20010000
		End	0x20017FFF	0x20017FFF	0x20017FFF	0x20017FFF
	SRAM B1	Start	0x20018000	0x20018000	0x20018000	0x20018000
		End	0x2001DFFF	0x2001DFFF	0x2001FFFF	0x2001FFFF
	SRAM C0	Start	—	—	0x20020000	0x20020000
		End	—	—	0x20027FFF	0x20027FFF
	SRAM C1	Start	—	—	0x20028000	0x20028000

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Table 6. SRAM and Flash address information...*continued*

Memory			MCX A175 MCX A185	MCX A255 MCX A265	MCX A176 MCX A186	MCX A256 MCX A266
		End	—	—	0x2002FFFF	0x2002FFFF
	SRAM C2	Start	—	—	0x20030000	0x20030000
		End	—	—	0x20037FFF	0x20037FFF
	SRAM C3	Start	—	—	0x20038000	0x20038000
		End	—	—	0x2003BFFF	0x2003BFFF
	SRAM X0 Alias [3]	Start	0x2001E000	0x2001E000	0x2003C000	0x2003C000
		End	0x2001FFFF	0x2001FFFF	0x2003DFFF	0x2003DFFF

[1] Users are recommended to place code in the code bus memory range to improve code execution performance.
[2] Customer Manufacturing/Factory Configuration Area (CMPA).
[3] SRAM X0 is enabled in Alias mode by default.

3 Ratings

3.1 Thermal handling ratings

Table 7. Thermal handling ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
TSTG	Storage temperature [1]	–55	—	150	°C	—
TSDR	Solder temperature, lead-free [2]	—	—	260	°C	—

[1] Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.
[2] Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

3.2 Moisture handling ratings

Table 8. Moisture handling ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
MSL	Moisture sensitivity level [1]	—	—	3	—	—

[1] Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

3.3 ESD handling ratings

Table 9. ESD handling ratings

Description	Rating	Unit	Notes
Electrostatic discharge voltage, human body model	+/-2000	V	[1]
Electrostatic discharge voltage, charged-device model	+/-500	V	[2]

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Table 9. ESD handling ratings...*continued*

Description	Rating	Unit	Notes
Electrostatic discharge voltage, charged device model (corner pins)	+/-750	V	[2]
Latch-up immunity level (Class II at 110 °C junction temperature)	Immunity Level A	—	[3]

[1] Determined according to ANSI/ESDA/JEDEC Standard JS-001-2023, For Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM) - Device Level.
[2] Determined according to ANSI/ESDA/JEDEC Standard JS-002-2022, For Electrostatic Discharge Sensitivity Testing, Charged Device Model (CDM) - Device Level.
[3] Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

3.4 Voltage and current maximum ratings

The table below shows the absolute minimum and maximum rating for the device. If the values are violated, device could be damaged. See Voltage and current for operating requirements, and Terminology and guidelines for definitions of terms.

Table 10. Voltage and current maximum ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	Supply voltage for Port 0, Port 1, Port 2, Port 3 and Port 4	-0.3	—	3.63	V	—
VDD_ANA	Supply voltage for ADC	-0.3	—	3.63	V	—
VDD_USB	Supply voltage for USB analog	-0.3	—	3.63	V	—
VUSB0_Dx	USB0_DP and USB0_DM input voltage	-0.3	—	3.63	V	—
VDIO	Digital input voltage	-0.3	—	VDD + 0.3	V	—
VDIO_5VTOL	Digital input voltage for 5V tolerant I/O pins	-0.3	—	min(VDD + 3.6V, 5.5V)	V	—
VAIO	Analog input voltage [1]	-0.3	—	VDD_ANA + 0.3	V	—
IDD	Digital supply current [2]	—	—	100	mA	—
ID	Maximum current single pin limit (digital output pins)	-25	—	25	mA	—

[1] Analog pins are defined as pins that do not have an associated general-purpose I/O port function.
[2] This limit is per supply pin. It includes all power pins, including VDD, VDD_ANA, VDD_USB.

3.5 Required Power-On-Reset (POR) Sequencing

- VDD and VDD_ANA must be same voltage

4 General

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4.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

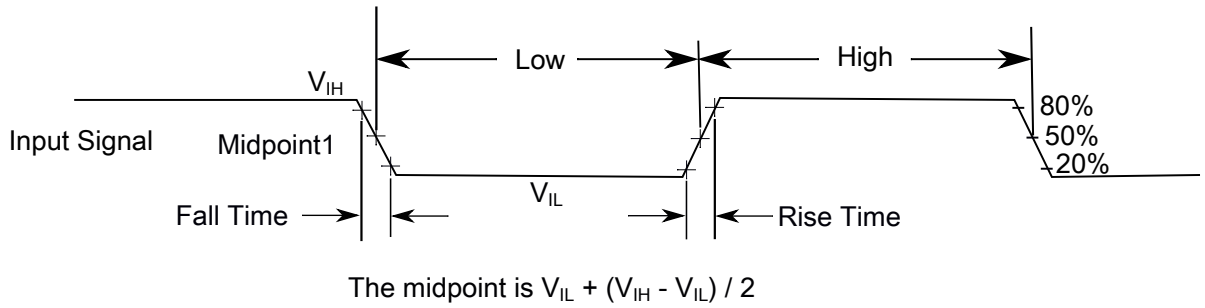


Figure 3. Input signal measurement reference

4.2 Nonswitching electrical specifications

4.2.1 Voltage and current operating requirement

Table 11. Voltage and current operating requirement

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	Supply Voltage for IO, LDO, Flash, and LPCMP	1.71	—	3.6	V	—
VDD_ANA	Supply voltage for ADC	VDD - 0.1	—	VDD + 0.1	V	—
VSS - VSS_ANA	VSS-to-VSS_ANA differential voltage	-0.1	—	0.1	V	—
VDD_USB	Supply voltage for USB analog	3.0	—	3.6	V	—
VIH	Input high voltage	0.7 × VDD	—	—	V	1.71 V ≤ VDD ≤ 3.6 V
VIH_5VTOL	Input high voltage of 5V tolerant IO	0.7 × VDD	—	—	V	1.71 V ≤ VDD ≤ 3.6 V
VIL	Input low voltage	—	—	0.3 × VDD	V	1.71 V ≤ VDD ≤ 3.6 V
VIL_5VTOL	Input low voltage of 5 V tolerant IO	—	—	0.3 × VDD	V	1.71 V ≤ VDD ≤ 3.6 V
VHYS	Input hysteresis	0.1 × VDD	—	—	V	—
VHYS_5VTOL	Input hysteresis of 5 V tolerant IO	0.1 × VDD	—	—	V	—
IICIO	IO pin DC injection current — per pin [1]	-3	—	—	mA	VIN < VSS-0.3 V (negative current injection)

Table continues on the next page...

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Table 11. Voltage and current operating requirement...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
IICIO	IO pin DC injection current — per pin [1]	—	—	3	mA	VIN > VDD+0.3 V (positive current injection)
IICcont	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins	-25	—	—	mA	Negative current injection
IICcont	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins	—	—	25	mA	Positive current injection
VODPU	Open drain pullup voltage level [2]	VDD	—	VDD	V	—

[1] All I/O pins are internally clamped to VSS and VDD through an ESD protection diode. If VIN is greater than VDD_MIN(=VSS-0.3 V) or is less than VDD_MAX(=VDD+ 0.3 V), then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = (-0.3 - VIN)/(-IICIOmin). The positive injection current limiting resistor is calculated as R=(VIN-VDD_MAX)/IICIOmax. The actual resistor should be an order of magnitude higher to tolerate transient voltages

[2] Open drain outputs must be pulled to whichever supply voltage corresponds to that IO, VDD as appropriate.

4.2.2 HVD, LVD, and POR operating requirements

The device includes low-voltage detection (LVD) and high-voltage detection (HVD) power supervisor circuits for following power supplies:

- VDD

4.2.2.1 VDD supply HVD, LVD, and POR Operating Requirements

Table 12. VDD supply HVD, LVD, and POR Operating Requirements

Symbol	Description	Min	Typ	Max	Unit	Condition
VHVDH_VDD	VDD Rising high-voltage detect threshold (HVD assertion)	3.730	3.810	3.890	V	—
VHVDH_HYS_VDD	VDD High-voltage inhibit reset/ recover hysteresis	—	38	—	mV	—
VLVDH_VDD	VDD Falling low-voltage detect threshold (LVD assertion) - high range	2.567	2.619	2.673	V	—
VLVDH_HYS_VDD	VDD Low-voltage inhibit reset/ recover hysteresis - high range	—	27	—	mV	—
VLVDL_VDD	VDD Falling low-voltage detect threshold (LVD assertion) - low range	1.618	1.651	1.684	V	—
VLVDL_HYS_VDD	VDD Low-voltage inhibit reset/ recover hysteresis - low range	—	16	—	mV	—

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4.2.3 Voltage and current operating behaviors

Table 13. Voltage and current operating behaviors

Symbol	Description	Min	Typ	Max	Unit	Condition
VOH	Output high voltage — Normal drive strength [1]	VDD – 0.5	—	—	V	2.7 V ≤ VDD ≤ 3.6 V, IOH = 4 mA
VOH	Output high voltage — Normal drive strength [1]	VDD – 0.5	—	—	V	1.71 V ≤ VDD < 2.7 V, IOH = 2.5 mA
VOH	Output high voltage — High drive strength [1][2]	VDD – 0.5	—	—	V	2.7 V ≤ VDD ≤ 3.6 V, IOH = 6 mA
VOH	Output high voltage — High drive strength [1][2]	VDD – 0.5	—	—	V	1.71 V ≤ VDD < 2.7 V, IOH = 3.75 mA
IOHT	Output high current total for all ports	—	—	100	mA	—
VOL	Output low voltage — Normal drive strength [1][3]	—	—	0.5	V	2.7 V ≤ VDD ≤ 3.6 V, IOL = 4 mA
VOL	Output low voltage — Normal drive strength [1][3]	—	—	0.5	V	1.71 V ≤ VDD < 2.7 V, IOL = 2.5 mA
VOL	Output low voltage — High drive strength [1][2][3]	—	—	0.5	V	2.7 V ≤ VDD ≤ 3.6 V, IOL = 6 mA
VOL	Output low voltage — High drive strength [1][2][3]	—	—	0.5	V	1.71 V ≤ VDD < 2.7 V, IOL = 3.75 mA
IOLT	Output low current total for all ports	—	—	100	mA	—
IIN	Input leakage current (per pin) for full temperature range [4]	—	0.02	1	µA	—
IIN	Input leakage current (per pin) at 25 °C [4]	—	0.001	0.025	µA	—
IOZ	Hi-Z (off-state) leakage current (per pin)	—	0.02	1	µA	—
RPU	Internal pullup resistors	33	50	75	kΩ	—
RPU (I3C)	Internal pullup resistors [5]	(VDD - 0.27 V)/3 mA	1.75	—	kΩ	—
RPD	Internal pulldown resistors	33	50	75	kΩ	—
RHPU	High-resistance pullup option (PCRx[PV] = 1) [6]	0.67	—	1.5	MΩ	—
RHPD	High-resistance pulldown option (PCRx[PV] = 1) [6]	0.67	—	1.5	MΩ	—
VBG	Bandgap voltage reference voltage	0.98	1.0	1.02	V	—

[1] For the HD pads, when setting DSE1=1, the IOH/IOL are four times higher at the same VOH/VOL.
[2] RESET_B pins are always configured in high drive mode
[3] Open drain outputs must be pulled to VDD
[4] Measured at VDD = 3.6 V.

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[5] Only I3C pins support this option
[6] Only tamper pins and RESET_B pins support this option.

4.2.4 On-chip regulator electrical specifications

4.2.4.1 LDO_CORE electrical specifications

Table 14. LDO_CORE electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	LDO_CORE input supply voltage	1.71	—	3.6	V	—
ILOAD	LDO_CORE max load current	—	—	96	mA	Over drive strength
ILOAD	LDO_CORE max load current	—	—	2	mA	Low drive strength
IDD	LDO_CORE current consumption	—	—	250	µA	Over drive strength
IDD	LDO_CORE current consumption	—	—	500	nA	Low drive strength
IINRUSH	LDO_CORE inrush current	—	—	10	mA	—

4.2.5 Power mode transition operating behaviours

All specifications in the following table assume this clock configuration:

- CPU clock = 45 MHz
- AHB clock = 45 MHz
- Clock source = FRO180M

4.2.5.1 Power mode transition operating behaviors

Table 15. Power mode transition operating behaviors

Symbol	Description	Min	Typ	Max	Unit	Condition
tPOR	After a POR event, amount of time to execution of the first instruction (measured from the point where VDD reach 1.8V) across the operating temperature range of the chip.[1][2]	—	2.94	2.98	ms	—
tSLEEP	Sleep → Active[1][2][3][4]	—	0.42	0.46	µs	—
tDSLEEP	Deep Sleep → Active [1][2][3][4]	—	9.01	10.31	µs	—
tPWDN	Power Down → Active [1][2][3][5]	—	18.84	22.15	µs	—
tDPWDN	Deep Power Down → Active [1][2][3][4]	—	1.57	1.59	ms	—

[1] Max value is mean+3 × sigma of tested values at the worst case of ambient temperature range and VDD 1.71 V to 3.6 V. Max values are based on characterization but not covered by test limits in production.
[2] Typical value is the average of values tested at Temperature=25 ℃ and VDD=3.3 V
[3] WFE used for low-power mode entry
[4] SPC->LPWKUP_DELAY[LPWKUP_DELAY] = 0x00 and the Core voltage level is configured as same level for Active and Low Power mode (SPC->ACTIVE_CFG[CORELDO_VDD_LVL]=SPC->LP_CFG[CORELDO_VDD_LVL] = 01b).
[5] SPC->LPWKUP_DELAY[LPWKUP_DELAY] = 0x5B and the Core voltage level is configured as different level for Active and Low Power mode (SPC->ACTIVE_CFG[CORELDO_VDD_LVL] = 01b for Active mode, SPC->LP_CFG[CORELDO_VDD_LVL] = 00b for Low Power mode)

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4.2.6 Power consumption operating behaviors

The maximum values stated in the following sections represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

4.2.6.1 Power consumption operating behaviors

When calculating the total MCU current consumption the following considerations should be made:

- Specifications below only include power for the MCU itself including VDD, VDD_ANA.
- VDD_USB current draw are not included
- On top of the device's IDD current consumption, external loads applied to pins of the device need to be considered

Table 16. Power consumption operating behaviors

Symbol	Description	Condition[1]	Typ	Unit
IDD_ACT_MD_1 [2]	1. CPU_CLK = 45 MHz from FRO180M. VDD_CORE = 1.0V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Flash is configured to LP mode; Cache enabled. 3. While(1) loop executing from internal flash.	25 °C	3.32	mA
		105 °C	5.78	mA
		125 °C	7.98	mA
IDD_ACT_MD_2	1. CPU_CLK = 45 MHz from FRO180M. VDD_CORE = 1.0V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled; Cache enabled. 3. While(1) loop executing from internal flash.	25 °C	3.68	mA
		105 °C	6.14	mA
		125 °C	8.38	mA
IDD_ACT_MD_CM_1	1. CPU_CLK = 45 MHz from FRO180M. VDD_CORE = 1.0V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Flash is configured to LP mode; Cache enabled. 3. Coremark executing from internal flash.	25 °C	4.09	mA
		105 °C	6.55	mA
		125 °C	8.74	mA
IDD_ACT_MD_CM_2	1. CPU_CLK = 45 MHz from FRO180M. VDD_CORE = 1.0V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled; Cache enabled. 3. Coremark executing from internal flash.	25 °C	4.45	mA
		105 °C	6.93	mA
		125 °C	9.15	mA
IDD_ACT_OD_1	1. CPU_CLK = 180 MHz from FRO180M. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Flash is configured to LP mode; Cache enabled. 3. While(1) loop executing from internal flash.	25 °C	13.76	mA
		105 °C	17.32	mA
		125 °C	20.43	mA
IDD_ACT_OD_2	1. CPU_CLK = 180 MHz from FRO180M. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled; Cache enabled. 3. While(1) loop executing from internal flash.	25 °C	15.13	mA
		105 °C	18.89	mA
		125 °C	21.99	mA
IDD_ACT_OD_CM_1	1. CPU_CLK = 180 MHz from FRO180M. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Flash is configured to LP mode; Cache enabled. 3. Coremark executing from internal flash.	25 °C	17.79	mA
		105 °C	21.45	mA
		125 °C	24.61	mA

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Table 16. Power consumption operating behaviors...*continued*

Symbol	Description	Condition[1]	Typ	Unit
IDD_ACT_OD_CM_2	1. CPU_CLK = 180 MHz from FRO180M. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled; Cache enabled. 3. Coremark executing from internal flash.	25 °C	18.88	mA
		105 °C	22.79	mA
		125 °C	25.94	mA
IDD_ACT_OD_3	1. CPU_CLK = 240 MHz from System PLL. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Cache enabled. 3. While(1) loop executing from internal flash.	25 °C	18.82	mA
		105 °C	22.66	mA
		125 °C	26.06	mA
IDD_ACT_OD_4	1. CPU_CLK = 240 MHz from System PLL. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled; Cache enabled. 3. While(1) loop executing from internal flash.	25 °C	20.1	mA
		105 °C	24.02	mA
		125 °C	27.46	mA
IDD_ACT_OD_CM_3	1. CPU_CLK = 240 MHz from System PLL. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Cache enabled. 3. Coremark executing from internal flash.	25 °C	24.08	mA
		105 °C	28.11	mA
		125 °C	31.58	mA
IDD_ACT_OD_CM_4	1. CPU_CLK = 240 MHz from System PLL. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled; Cache enabled. 3. Coremark executing from internal flash.	25 °C	25.37	mA
		105 °C	29.45	mA
		125 °C	32.97	mA
IDD_ACT_OD_5	1. CPU_CLK = 240 MHz from FRO180M in 240 MHz mode. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Cache enabled. 3. While(1) loop executing from internal flash.	25 °C	17.58	mA
		105 °C	21.87	mA
		125 °C	25.55	mA
IDD_ACT_OD_6	1. CPU_CLK = 240 MHz from FRO180M in 240 MHz mode. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Cache enabled. 3. While(1) loop executing from internal flash.	25 °C	23.31	mA
		105 °C	27.79	mA
		125 °C	31.61	mA
IDD_ACT_OD_CM_5	1. CPU_CLK = 240 MHz from FRO180M in 240 MHz mode. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Cache enabled. 3. While(1) loop executing from internal flash.	25 °C	18.94	mA
		105 °C	23.31	mA
		125 °C	27.03	mA
IDD_ACT_OD_CM_6	1. CPU_CLK = 240 MHz from FRO180M in 240 MHz mode. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Cache enabled. 3. While(1) loop executing from internal flash.	25 °C	24.69	mA
		105 °C	29.21	mA
		125 °C	33.02	mA

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Table 16. Power consumption operating behaviors...*continued*

Symbol	Description	Condition[1]	Typ	Unit
IDD_SLEEP_OD_1	1. CPU_CLK = OFF; SYSTEM_CLK = 180 MHz from FRO180M. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled. 3. Core in WFI.	25 °C	8.08	mA
		105 °C	11.68	mA
		125 °C	14.75	mA
IDD_SLEEP_OD_2	1. CPU_CLK = OFF; SYSTEM_CLK = 180 MHz from FRO180M. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled. 3. Core in WFI.	25 °C	9.16	mA
		105 °C	12.69	mA
		125 °C	15.78	mA
IDD_SLEEP_MD_1	1. CPU_CLK = OFF; SYSTEM_CLK = 45 MHz from FRO180M. VDD_CORE = 1.0V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled. 3. Core in WFI.	25 °C	2.16	mA
		105 °C	4.59	mA
		125 °C	6.81	mA
IDD_SLEEP_MD_2	1. CPU_CLK = OFF; SYSTEM_CLK = 45 MHz from FRO180M. VDD_CORE = 1.0V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled. 3. Core in WFI.	25 °C	2.41	mA
		105 °C	4.85	mA
		125 °C	7.07	mA
IDD_SLEEP_MD_3	1. CPU_CLK = OFF; SYSTEM_CLK = 12 MHz from FRO12M. VDD_CORE = 1.0 V from LDO_CORE Low Drive. 2. All peripheral clocks disabled. 3. Core in WFI.	25 °C	0.579	mA
		105 °C	3.04	mA
		125 °C	5.32	mA
IDD_DEEP_SLEEP_OD_1	1. CPU_CLK = OFF; SYSTEM_CLK = OFF; SLOW_CLK = OFF; VDD_CORE = 1.2 V from LDO_CORE Normal Drive; FRO12M disabled. 2. All peripheral clocks disabled; all on-chip SRAM in deep sleep. 3. Core in WFI.	25 °C	542.27	µA
		105 °C	3000	µA
		125 °C	5130	µA
IDD_DEEP_SLEEP_MD_1	1. CPU_CLK = OFF; SYSTEM_CLK = OFF; SLOW_CLK = OFF; VDD_CORE = 1.0 V from LDO_CORE Low Drive; FRO12M disabled. 2. All peripheral clocks disabled; all on-chip SRAM in deep sleep. 3. Core in WFI.	25 °C	96.02	µA
		105 °C	1850	µA
		125 °C	3470	µA
IDD_DEEP_SLEEP_MD_2	1. CPU_CLK = OFF; SYSTEM_CLK = OFF; SLOW_CLK = OFF; VDD_CORE = 1.0 V from LDO_CORE Low Drive; FRO12M enabled. 2. All peripheral clocks disabled; all on-chip SRAM in deep sleep. 3. Core in WFI.	25 °C	155.29	µA
		105 °C	1910	µA
		125 °C	3530	µA
IDD_POWER_DOWN_1	1. CPU_CLK = SYSTEM_CLK = OFF; VDD_CORE = 0.6V retention voltage from LDO_CORE Low Drive 2. All RAM retained; FRO16K disabled. 3. Core in WFI.	25 °C	31.95	µA
		105 °C	915.38	µA
		125 °C	1810	µA
IDD_DEEP_POWER_DOWN_1	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. All RAM OFF; Wake timer disabled, FRO16K disabled. 3. Core in WFI.	25 °C	0.473	µA
		105 °C	7.95	µA
		125 °C	18.62	µA

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Table 16. Power consumption operating behaviors...*continued*

Symbol	Description	Condition[1]	Typ	Unit
IDD_DEEP_POWER_DOWN_2	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. All RAM OFF; Wake timer enabled, FRO16K enabled. 3. Core in WFI.	25 °C	0.646	µA
		105 °C	8.15	µA
		125 °C	18.76	µA
IDD_DEEP_POWER_DOWN_3	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. All RAM retained; Wake timer enabled, FRO16K enabled. 3. Core in WFI.	25 °C	3.4	µA
		105 °C	83.13	µA
		125 °C	183.28	µA
IDD_DEEP_POWER_DOWN_4	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. RAM X0/X1/B0/B1, A0~A4 retained; Wake timer enabled, FRO16K enabled. 3. Core in WFI.	25 °C	2.29	µA
		105 °C	50.43	µA
		125 °C	110.66	µA
IDD_DEEP_POWER_DOWN_5	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. RAM X0/X1/B0/B1/A0 retained; Wake timer enabled, FRO16K enabled. 3. Core in WFI.	25 °C	1.66	µA
		105 °C	33.49	µA
		125 °C	74.02	µA
IDD_DEEP_POWER_DOWN_6	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. RAM A0 retained; Wake timer enabled, FRO16K enabled. 3. Core in WFI.	25 °C	0.849	µA
		105 °C	11.41	µA
		125 °C	25.7	µA
IDD_DEEP_POWER_DOWN_7	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. RAM X0/X1/B0/B1 retained; Wake timer enabled, FRO16K enabled. 3. Core in WFI.	25 °C	1.55	µA
		105 °C	30.39	µA
		125 °C	67.28	µA
IDD_DEEP_POWER_DOWN_8	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. RAM A0 retained; RTC enabled, Wake timer disabled, FRO16K enabled. 3. Core in WFI.	25 °C	0.842	µA
		105 °C	11.44	µA
		125 °C	25.76	µA
IDD_DEEP_POWER_DOWN_9	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. RAM A0 retained; RTC enabled, Wake timer enabled, FRO16K enabled. 3. Core in WFI.	25 °C	0.855	µA
		105 °C	11.43	µA
		125 °C	25.73	µA
IDD_DEEP_POWER_DOWN_10	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. All RAM OFF; RTC enabled, Wake timer disabled, FRO16K enabled. 3. Core in WFI.	25 °C	0.651	µA
		105 °C	8.11	µA
		125 °C	18.77	µA
IDD_DEEP_POWER_DOWN_11	1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. All RAM OFF; RTC enabled, Wake timer disabled, FRO16K enabled, Digital Tamper (TDET) enabled. 3. Core in WFI.	25 °C	0.727	µA
		105 °C	8.21	µA
		125 °C	18.83	µA

[1] Ambient temperature
[2] MD middle drive, core voltage is 1.0V. OD over drive, core voltage is 1.2V

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4.2.7 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

4.2.8 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to nxp.com.
2. Perform a keyword search for “EMC design”.

4.2.9 Capacitance attributes

Table 17. Capacitance attributes

Symbol	Description	Min	Typ	Max	Unit	Condition
CIN_A	Input capacitance: analog pins	—	—	7	pF	—
CIN_D	Input capacitance: digital pins	—	—	7	pF	—

4.3 Switching specifications

4.3.1 Device clock specs

Table 18. Device clock specs

Symbol	Description	Min	Typ	Max	Unit	Condition
fCPU	CPU clock (CPU_CLK)For MCXA185/186/265/266	—	—	240	MHz	Over drive (OD) mode, VDD_CORE = 1.2 V
fSYSTEM	System clock (SYSTEM_CLK)For MCXA185/186/265/266	—	—	240	MHz	Over drive (OD) mode, VDD_CORE = 1.2 V
fSLOW	Slow clock (SLOW_CLK)For MCXA185/186/265/266	—	—	40	MHz	Over drive (OD) mode, VDD_CORE = 1.2 V
fCPU	CPU clock (CPU_CLK)For MCXA175/176/255/256	—	—	180	MHz	Over drive (OD) mode, VDD_CORE = 1.2 V
fSYSTEM	System clock (SYSTEM_CLK)For MCXA175/176/255/256	—	—	180	MHz	Over drive (OD) mode, VDD_CORE = 1.2 V
fSLOW	Slow clock (SLOW_CLK)For MCXA175/176/255/256	—	—	30	MHz	Over drive (OD) mode, VDD_CORE = 1.2 V
fCPU	CPU clock (CPU_CLK)	—	—	45	MHz	Middle drive (MD) mode VDD_CORE = 1.0 V
fSYSTEM	SYSTEM clock (SYSTEM_CLK)	—	—	45	MHz	Middle drive (MD) mode VDD_CORE = 1.0 V
fSLOW	Slow clock (SLOW_CLK)	—	—	7.5	MHz	Middle drive (MD) mode VDD_CORE = 1.0 V

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4.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO, LPUART, LPI2C, LPI3C, LPSPI functions.

4.3.2.1 General switching specifications

Note: *Refer to the pinout spreadsheet.*

Table 19. General switching specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
—	GPIO pin interrupt pulse width — Synchronous path [1]	1.5	—	—	SYSTEM clock cycles	The synchronous and asynchronous timing must be met.
—	GPIO pin interrupt pulse width — Asynchronous path	150	—	—	ns	—
—	GPIO pin interrupt pulse width — Asynchronous path	50	—	—	ns	—
—	External RST pin interrupt pulse width — Asynchronous path [2]	330	—	—	ns	This is the shortest pulse that is guaranteed to be recognized.
—	GPIO pin interrupt pulse width — Asynchronous path [2]	16	—	—	ns	—
—	Port rise/fall time for slow I/O pins [3][4]	1	—	7	ns	2.7 ≤ VDD ≤ 3.6 V, Fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for slow I/O pins [3][4]	3.5	—	15	ns	2.7 ≤ VDD≤ 3.6 V, Slow slew rate (SRE = 1; DSE = 0)
—	Port rise/fall time for slow I/O pins [3][4]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, Fast slew rate (SRE = 0; DSE = 1)
—	Port rise/fall time for slow I/O pins [3][4]	3.5	—	25	ns	1.71 ≤ VDD < 2.7 V, Slow slew rate (SRE = 1; DSE = 1)
—	Port rise/fall time for slow I/O pins, 5V Tolerant [3][4]	1	—	7	ns	2.7 ≤ VDD ≤ 3.6 V, Fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for slow I/O pins, 5V Tolerant [3][4]	3.5	—	15	ns	2.7 ≤ VDD≤ 3.6 V, Slow slew rate (SRE = 1; DSE = 0)
—	Port rise/fall time for slow I/O pins, 5V Tolerant [3][4]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, Fast slew rate (SRE = 0; DSE = 1)
—	Port rise/fall time for slow I/O pins, 5V Tolerant [3][4]	3.5	—	25	ns	1.71 ≤ VDD < 2.7 V, Fast slew rate (SRE = 1; DSE = 1)

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Table 19. General switching specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Port rise/fall time for medium I/O pins [5][6]	0.8	—	4	ns	2.7 ≤ VDD ≤ 3.6 V, Fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for medium I/O pins [5][6]	1	—	7	ns	2.7 ≤ VDD ≤ 3.6 V, Slow slew rate (SRE = 1; DSE = 0)
—	Port rise/fall time for medium I/O pins [5][6]	0.8	—	4	ns	1.71 ≤ VDD < 2.7 V, Fast slew rate (SRE = 0; DSE = 1)
—	Port rise/fall time for medium I/O pins [5][6]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, Slow slew rate (SRE = 1; DSE = 1)
—	HD pins [7]	2.2	—	7	ns	2.7 ≤ VDD≤ 3.6 V, Normal drive, fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for HD pins [7]	1	—	7	ns	2.7 ≤ VDD≤ 3.6 V, Normal drive (DSE = 0), fast slew rate (SRE = 0)
—	Port rise/fall time for HD pins [7]	3.5	—	15	ns	2.7 ≤ VDD ≤ 3.6 V, Normal drive (DSE =0), slow slew rate (SRE = 1)
—	Port rise/fall time for HD pins [7]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, High drive (DSE=1), Fast slew rate (SRE = 0)
—	Port rise/fall time for HD pins [7]	3.5	—	25	ns	1.71 ≤ VDD < 2.7 V, High drive (DSE =1), Slow slew rate (SRE=1)
—	RST pins [4]	3	—	8	ns	2.7 ≤ VDD ≤ 3.6 V
—	RST pins [4]	3.6	—	20	ns	1.71 ≤ VDD < 2.7 V

[1] The synchronous and asynchronous timing must be met.
[2] This is the shortest pulse that is guaranteed to be recognized
[3] For the HD I/O pins, setting DSE1 = 1 will support the same rise/fall time at 4x the load capacitance. For the 5VTOL I/O pins, setting DSE1=1 will support the same fall time at 2x the load capacitance, but the rise time will increase due to the increased loading
[4] Load is 25 pF.
[5] Assumes default values in CALIB1 and CALIB0 in PORTS
[6] 25 pF lumped load
[7] Load is 25 pF for DSE=0. Load is 100 pF for DSE=2 or DSE=3. Drive strength and slew rate are configured using PORTx_PCRn[DSE1], PORTx_PCRn[DSE], and PORTx_PCRn[SRE].

4.4 Thermal specifications

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4.4.1 Thermal operating requirements

Table 20. Thermal operating requirements

Symbol	Description	Min	Typ	Max	Unit	Condition
TA	Ambient temperature [1]	-40	25	125	°C	—
TJ	Die junction temperature [2][3][4]	—	—	125	°C	—

[1] The device may operate at maximum TA rating as long as TJ maximum of 125 °C is not exceeded. The simplest method to determine TJ is: TJ = TA + RθJA*chip power dissipation.
[2] The device operating specification is not guaranteed beyond 125 °C TJ.
[3] The maximum operating requirement applies to all chapters unless otherwise specifically stated.
[4] Operating at maximum conditions for extended periods may affect device reliability. Refer to Product Lifetime Usage Estimates application note (AN14194)

4.4.2 Thermal attributes

Table 21. Thermal attributes

Rating	Board Type[1]	Symbol	LQFP64	LQFP100	LQFP144	WFBGA169	Unit
Junction to Ambient Thermal Resistance [2]	2s2p	$R_{\theta JA}$	34.5	45.3	41.9	48.2	°C/W
Junction-to-Top of Package Thermal Characterization Parameter [2]	2s2p	Ψ_{JT}	2.2	0.7	1.3	1.6	°C/W
Junction to Case Top Thermal Resistance [3]	1s	$R_{\theta JC}$	18.9	15.4	14.5	19.2	°C/W

[1] Thermal test board meets JEDEC specification for this package (JESD51-9 for non-leaded package(BGA) while JESD 51-7 is for leaded package(QFN,QFP,SOIC))
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment
[3] Junction-to-Case thermal resistance determined using an isothermal cold plate. For QFN package, case temperature refers to the exposed pad surface temperature at the package bottom side dead centre. For QFP/BGA packages, case temperature refers to the mold surface temperature at the package top side dead centre..

5 Peripheral operating requirements and behaviors

5.1 Core modules

5.1.1 JTAG debug interface timing

The following table lists JTAG specifications in Debug Interface mode.

Table 22. JTAG debug interface timing

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Operating voltage	1.71	—	3.6	V	—
J1	TCLK frequency of operation	—	—	25	MHz	Boundary Scan (OD mode)
J1	TCLK frequency of operation	—	—	12.5	MHz	Boundary Scan (MD mode)

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Table 22. JTAG debug interface timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
J1	TCLK frequency of operation	—	—	25	MHz	JTAG-DP/TAP (OD mode)
J1	TCLK frequency of operation	—	—	12.5	MHz	JTAG-DP/TAP
J2	TCLK cycle period	1000/J1	—	—	ns	—
J3	TCLK clock pulse width	J2/2	—	—	ns	—
J4	TCLK rise and fall times	—	—	3	ns	—
J5	Boundary scan input data setup time to TCLK rise	—	—	8	ns	OD mode
J5	Boundary scan input data setup time to TCLK rise	—	—	16	ns	MD mode
J6	Boundary scan input data hold time after TCLK rise	1	—	—	ns	OD mode
J6	Boundary scan input data hold time after TCLK rise	1	—	—	ns	MD mode
J7	TCLK low to boundary scan output data valid	—	—	18	ns	OD mode
J7	TCLK low to boundary scan output data valid	—	—	38	ns	MD mode
J8	TCLK low to boundary scan output high-Z	—	—	18	ns	OD mode
J8	TCLK low to boundary scan output high-Z	—	—	38	ns	MD mode
J9	JTAG-DP/TAP TMS, TDI input data setup time to TCLK rise	—	—	8	ns	OD mode
J9	JTAG-DP/TAP TMS, TDI input data setup time to TCLK rise	—	—	16	ns	MD mode
J10	JTAG-DP/TAP TMS, TDI input data hold time after TCLK rise	1	—	—	ns	OD mode
J10	JTAG-DP/TAP TMS, TDI input data hold time after TCLK rise	1	—	—	ns	MD mode
J11	TCLK low to JTAG-DP/TAP TDO data valid	—	—	18	ns	OD mode
J11	TCLK low to JTAG-DP/TAP TDO data valid	—	—	38	ns	MD mode
J12	TCLK low to JTAG-DP/TAP TDO high-Z	—	—	18	ns	OD mode
J12	TCLK low to JTAG-DP/TAP TDO high-Z	—	—	38	ns	MD mode

TDOC represents the TDO bit frame of the scan packet in compact JTAG 2-wire mode.

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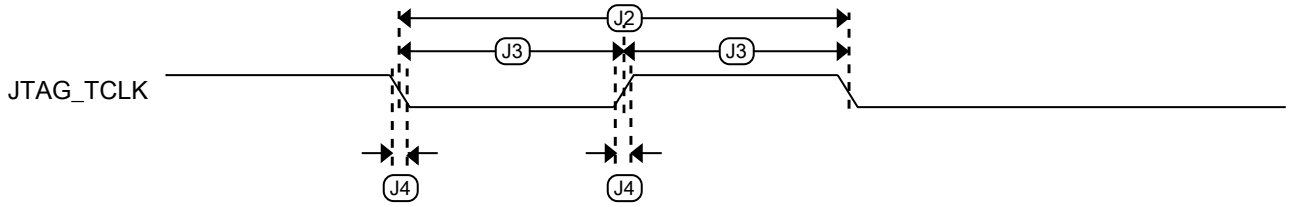


Figure 4. Test clock input timing

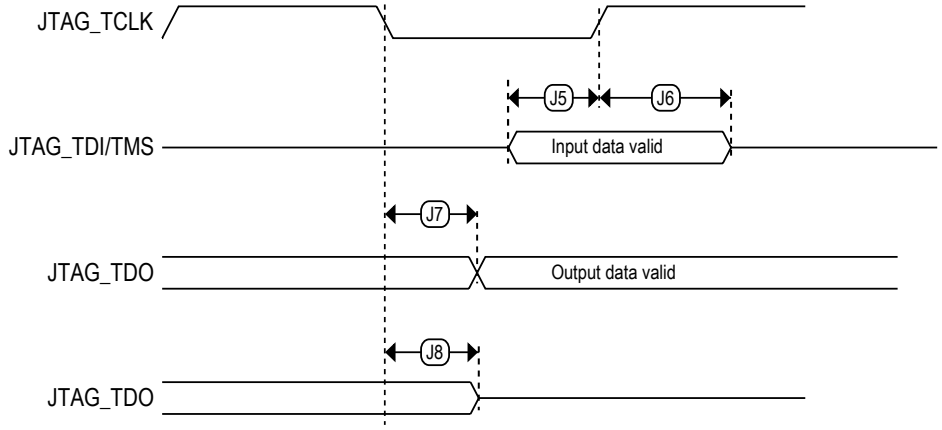


Figure 5. Boundary scan (JTAG) timing

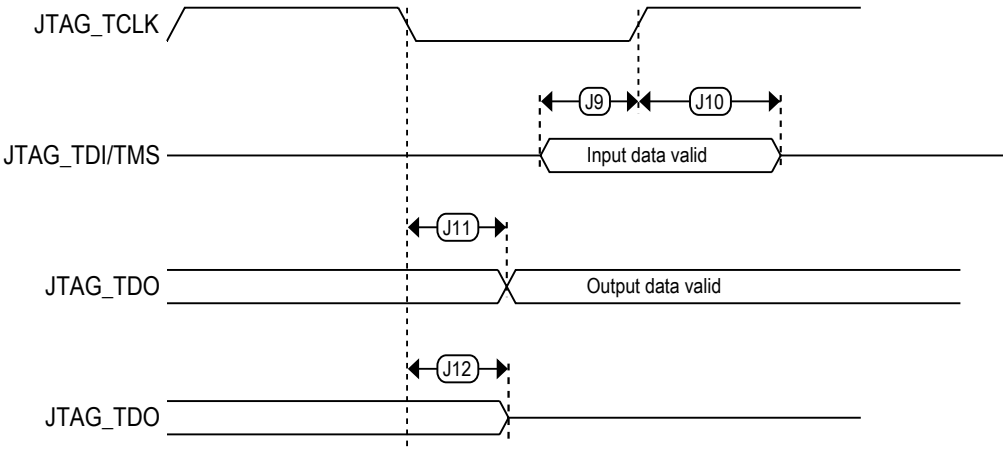


Figure 6. JTAG-DP/TAP timing

5.1.2 Serial Wire Debug (SWD) Timing

The following table gives the Serial Wire Debug specifications for the device.

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Table 23. Serial Wire Debug (SWD) Timing

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Operating voltage	1.71	—	3.6	V	—
S1	SWD_CLK frequency of operation	—	—	25	MHz	OD mode
S1	SWD_CLK frequency of operation	—	—	20	MHz	MD mode
S2	SWD_CLK cycle period	1000/S1	—	—	ns	OD mode
S2	SWD_CLK cycle period	1000/S1	—	—	ns	MD mode
S3	SWD_CLK clock pulse width	20	—	—	ns	OD mode
S3	SWD_CLK clock pulse width	25	—	—	ns	MD mode
S4	SWD_CLK rise and fall times	—	—	3	ns	—
S5	SWD_DIO input data setup time to SWD_CLK rise	—	—	10	ns	OD mode
S5	SWD_DIO input data setup time to SWD_CLK rise	—	—	12.5	ns	MD mode
S6	SWD_DIO input data hold time after SWD_CLK rise	0	—	—	ns	OD mode
S6	SWD_DIO input data hold time after SWD_CLK rise	0	—	—	ns	MD mode
S7	SWD_CLK high to SWD_DIO data valid	—	—	25	ns	OD mode
S7	SWD_CLK high to SWD_DIO data valid	—	—	30	ns	MD mode
S8	SWD_CLK high to SWD_DIO high-Z	—	—	25	ns	OD mode
S8	SWD_CLK high to SWD_DIO high-Z	—	—	30	ns	MD mode

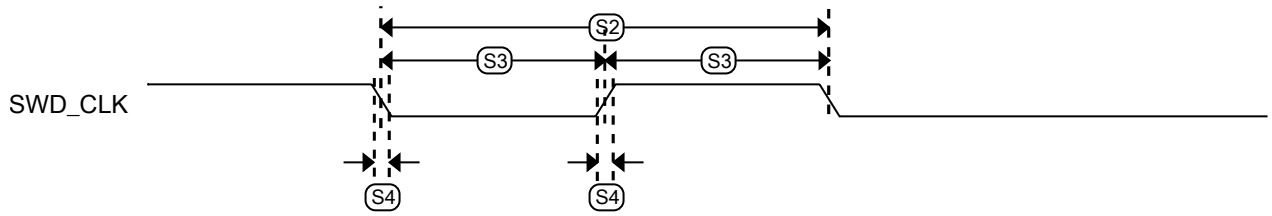


Figure 7. Serial Wire clock input timing

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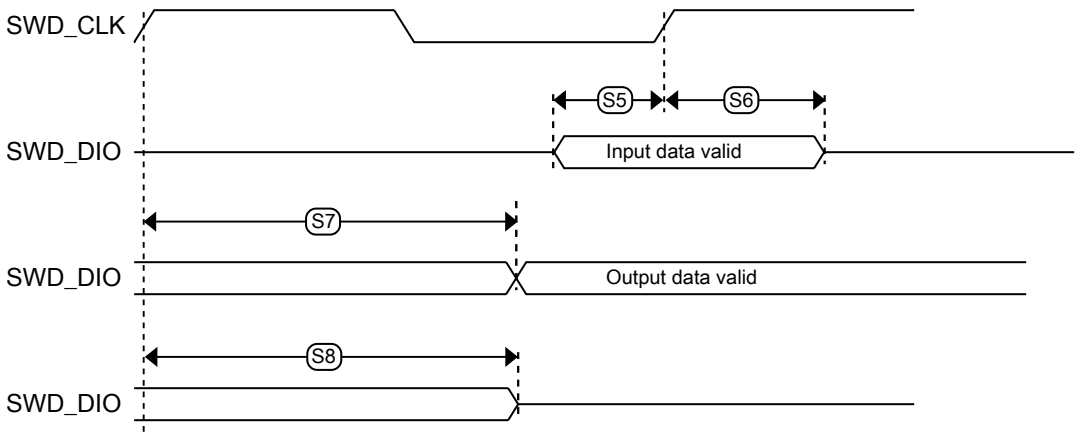


Figure 8. Serial Wire data timing

5.2 Clock modules

5.2.1 Reference Oscillator Specification

This chip is designed to meet targeted specifications with a ±40 ppm frequency error over the life of the part, which includes the temperature, mechanical, and aging excursions.

The table below shows typical specifications for the Crystal Oscillator.

5.2.1.1 System oscillator crystal specifications

Table 24. System oscillator crystal specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
fosc	Crystal frequency	8	—	50	MHz	—
Tol	Frequency tolerance	—	±10	±40	ppm	—
Jitosc	Jitter	—	70	—	—	Period jitter (RMS)
Vpp	Peak-to-peak amplitude of oscillation [1]	—	0.6	—	V	—
fec	Externally provided input clock frequency [2]	0	—	50	MHz	—
tDC_EXTAL	External clock duty cycle	45	50	55	%	—
Vec	Externally provided input clock amplitude	Refer to VIH and VIL specification	—	—	—	—
Cin	Parasitic capacitance of EXTAL	—	2	8	pF	—
Cout	Parasitic capacitance of XTAL	—	2	10	pF	—
tstart	Crystal start-up time [3]	—	186	—	µs	Normal mode fcrystal = 16 MHz, Rm = 200 Ω,

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Table 24. System oscillator crystal specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
						Cp = 1 pF, Cload = 8 pF, Cm = 0.008 pF, Lm = 12.37 mH
IOSC	Current consumption	—	200	—	µA	Normal mode fcrystal = 16 MHz, Rm = 200 Ω, Cp = 1 pF, Cload = 8 pF, Cm=0.008 pF, Lm = 12.37 mH
IOSC	Current consumption	—	—	3	µA	Disable mode

[1] When a crystal is being used with the oscillator, the EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.
[2] This specification is for an externally supplied clock driven to EXTAL and does not apply to any other clock input.
[3] Dependent on crystal specifications, proper PC board layout procedures must be followed to achieve specifications

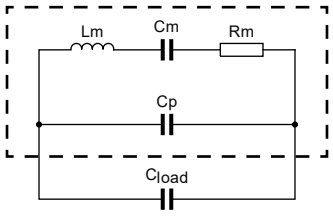


Figure 9. Crystal Electrical Block Diagram

5.2.1.2 System oscillator crystal examples

Table 25. System oscillator crystal examples

Freq Crystal (MHz)	R_m(Ω)	C_p(pF)	C_{load}(pF)	C_m(pF)	L_m(mH)	Typical startup (µs)[1]	Typical Current consumption (µA)[1]	Drive level (µW)	
								min	max
8	100	5.00	18.0	0.008	49.47	1240	168	24	34
16	80	2.00	8.00	0.008	12.37	215	168.3	16	22
16	200	1.00	8.00	0.008	12.37	186	200.4	31	46
25	60	3.00	11.0	0.008	5.07	224	245.6	70	93
25	60	2.00	10.0	0.008	5.07	128	232.5	61	80
25	100	1.00	8.00	0.008	5.07	73.6	232.7	62	82
32	60	3.00	9.00	0.008	3.09	233	269.6	71	95
32	60	2.00	8.00	0.008	3.09	116	253.2	59	80
32	100	1.00	8.00	0.008	3.09	52.4	289.3	91	123
40	50	2.00	8.00	0.008	1.98	80.4	296.9	73	99

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Table 25. System oscillator crystal examples *...continued*

40	60	3.00	9.00	0.008	1.98	162	333.2	99	135
48	50	2.00	8.00	0.008	1.37	73.1	359.6	104	140
48	60	3.00	9.00	0.008	1.37	155	407.9	138	188

[1] This is based on simulation

5.2.2 FRO180M specifications

Table 26. FRO180M specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
jitper	Period jitter RMS [1]	—	70	—	ps	—
jitper	Accumulated jitter over 10K cycles [1]	—	800	—	ps	—
Ivdda	3.3V analog supply current	—	50	—	µA	—
Ivdd	1.1 V analog supply current	—	58	—	µA	—
Ivdda_dis	3.3 V leakage current	—	5	—	nA	—
Ivdd_dis	1.1 V leakage current	—	40	—	nA	—
fclkout	Clock frequency [2][3]	—	45/45	—	MHz	freq_sel[2:0]=3'b001, set the FRO180M trim to 180 MHz
fclkout	Clock frequency [2][3]	—	60/45	—	MHz	freq_sel[2:0]=3'b011, set the FRO180M trim to 180 MHz
fclkout	Clock frequency [2][3]	—	90/45	—	MHz	freq_sel[2:0]=3'b101, set the FRO180M trim to 180 MHz
fclkout	Clock frequency [2][3]	—	180/45	—	MHz	freq_sel[2:0]=3'b111, set the FRO180M trim to 180 MHz
fclkout	Clock frequency [2][3]	—	60/60	—	MHz	freq_sel[2:0]=3'b001, set the FRO180M trim to 240 MHz
fclkout	Clock frequency [2][3]	—	80/60	—	MHz	freq_sel[2:0]=3'b011, set the FRO180M trim to 240 MHz
fclkout	Clock frequency [2][3]	—	120/60	—	MHz	freq_sel[2:0]=3'b101, set the FRO180M trim to 240 MHz
fclkout	Clock frequency [2][3]	—	240/60	—	MHz	freq_sel[2:0]=3'b111, set the FRO180M trim to 240 MHz

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Table 26. FRO180M specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
Δfclkout	Frequency variation for packages other than WFBGA169 [4]	-1	—	1	%	-40 °C ≤ TJ ≤ 125 °C
Δfclkout	Frequency variation for WFBGA169 package [4]	-1.5	—	1	%	0 °C ≤ TJ ≤ 85 °C
Δfclkout	Frequency variation for WFBGA169 package [4]	-2	—	1	%	-40 °C ≤ TJ ≤ 85 °C
Δfclkout	Frequency variation for WFBGA169 package [4]	-5	—	1	%	-40 °C ≤ TJ ≤ 125 °C
fclkout_closeloop	Close loop accuracy with autotrim from an accurate clock source	-0.25	—	0.25	%	—
tstartup	Start-up time from disable to 20% accuracy	—	2	—	µs	—
tsettle	Settling time from disable to 1% accuracy	—	—	50	µs	—
fovershoot	frequency overshoot during start-up and settling	—	—	2	%	—
DC	Duty cycle of the clock	45	—	55	%	—

[1] Tested at 80 MHz
[2] Frequency in left of slash is fro-hf, and frequency in right of slash is clk_45m in reference manual clocking chapter
[3] Guaranteed by design
[4] Characterization on a production tester

5.2.3 FRO12M specifications

Table 27. FRO12M specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
ffro12m	FRO12M frequency (nominal)	—	12	—	MHz	—
Δffro12m	Frequency deviation	—	—	±3	%	open loop
Δffro12m	Frequency deviation	—	—	±0.6	%	closed loop (using accurate clock source as reference)
tstartup	Start-up time	—	5	—	µs	—
fos	Frequency overshoot during startup	—	10	20	%	—
Ifro12m	Current consumption	—	7	—	µA	—

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5.2.4 FRO16K specifications

Table 28. FRO16K specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
ffro16k	FRO16K frequency (nominal) [1]	—	16.384	—	kHz	—
Δffro16k	Frequency variation for package other than WFBGA169	-6	—	6	%	open loop, –40 °C ≤ TJ ≤ 125 °C
Δffro16k	Frequency variation for WFBGA169 package [2]	-9	—	6	%	open loop, –40 °C ≤ TJ ≤ 125 °C
TRIMstep	Trimming step	—	1.5	—	%	—
tstartup	Start-up time	—	310	—	µs	—
Ifro16k	Current consumption	—	50	—	nA	—

[1] Guaranteed by design
[2] Characterization on a production tester

5.2.5 550 MHz PLL electrical specifications

Table 29. 550 MHz PLL electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
fcco	CCO operating frequency	275	—	550	MHz	—
Ipll	PLL operating current	—	484	—	µA	fcco = 550 MHz and fout = 55 MHz
fref	PLL reference frequency range	5	—	150	MHz	—
Jpp_period	Peak-Peak period jitter	—	110	—	ps	Fref = 12 MHz, fcco = 550 MHz, fvco = 550 MHz
Jrms_int	RMS interval jitter	—	14	—	ps	fout = fcco = 550 MHz, fref = 12 MHz
tpon	Start-up time	—	—	500 + 300/Fref	µs	—

Note: The PLL is only available in OD mode and cannot be used in MD mode.

5.3 Memories and memory interfaces

5.3.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

5.3.1.1 Timing specifications

The following command times assume a flash bus clock frequency of 24 MHz. Command times will be increased by up to 10 µs at 24 MHz if the module is exiting sleep mode when the command is launched. The time to abort a command is not included in the following table.

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5.3.1.1.1 Flash command time specifications

Table 30. Flash command time specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
trd1all256k	Read 1s All execution time (256 KB)	—	—	1700	µs	—
trd1all512k	Read 1s All execution time (512 KB)	—	—	3200	µs	—
trd1all1MB	Read 1s All execution time (1 MB)	—	—	6200	µs	—
trd1blk256k	Read 1s Block execution time (256 KB)	—	—	1500	µs	—
trd1blk512k	Read 1s Block execution time (512KB)	—	—	3050	µs	—
trd1blk1MB	Read 1s Block execution time (1MB)	—	—	6000	µs	—
trd1scr	Read 1s Sector execution time (8 KB) [1]	—	—	50	µs	—
trd1pg	Read 1s Page execution time (128 B) [1]	—	—	4.4	µs	—
trd1pglv	Read 1s Page at low voltage execution time (128 B)	—	—	5.8	µs	—
trd1phr	Read 1s Phrase execution time (16B) [1]	—	—	3.8	µs	—
trd1phrlv	Read 1s Phrase at low voltage execution time (16 B)	—	—	4.8	µs	—
trdmisr8k	Read into MISR (8 KB) [1]	—	—	50	µs	—
trdmisr256k	Read into MISR (256 KB)	—	—	1500	µs	—
trdmisr512k	Read into MISR (512 KB)	—	—	3050	µs	—
trdmisr1M	Read into MISR (1 MB) [1]	—	—	6000	µs	—
trd1ipg	Read 1s IFR Page execution time (128 B) [1]	—	—	4.4	µs	—
trd1ipglv	Read 1s IFR Page at low voltage execution time (128 B)	—	—	5.8	µs	—
trd1iphr	Read 1s IFR Phrase execution time (16 B) [1]	—	—	3.8	µs	—
trd1iphrlv	Read 1s IFR Phrase at low voltage execution time (16 B)	—	—	4.8	µs	—
trdimisr8k	Read IFR into MISR (8 KB) [1]	—	—	50	µs	—
trdimisrk32k	Read IFR into MISR (32 KB) [1]	—	—	190	µs	—

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Table 30. Flash command time specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tpgmpg_initial	Program Page execution time at < 1k cycles (128 B) [2]	—	450	600	µs	—
tpgmpg_lifetime	Program Page execution time at > 1k cycles (128 B)	—	450	750	µs	—
tpgmphr_initial	Program Phrase execution time at < 1k cycles (16 B) [2]	—	135	180	µs	—
tpgmphr_lifetime	Program Phrase execution time at > 1k cycles (16 B)	—	135	225	µs	—
tersall256k	Erase All execution time (256 KB)	—	—	800	ms	—
tersall512k	Erase All execution time (512 KB)	—	—	1500	ms	—
tersall1M	Erase All execution time (1 MB)	—	—	2800	ms	—
tmasers256k	Mass Erase execution time (via sideband) (256 KB)	—	—	800	ms	—
tmasers512k	Mass Erase execution time (via sideband) (512 KB)	—	—	1500	ms	—
tmasers1M	Mass Erase execution time (via sideband) (1 MB)	—	—	2800	ms	—
terrscr	Erase Sector execution time (8 KB) [2]	—	2	22	ms	—

[1] Time to abort the command may significantly impact the time to execute the command.
[2] Measured from the time FSTAT[PERDY] is cleared.

5.3.1.2 Flash high voltage current behavior

Table 31. Flash high voltage current behavior

Symbol	Description	Min	Typ	Max	Unit	Condition
IDD_IO_PGM	Average current adder to VDD during flash programming operation [1]	—	—	6	mA	—
IDD_IO_ERS	Average current adder to VDD during flash erase operation [1]	—	—	4	mA	—

[1] See the Power Management chapter in the reference manual for the specific VDD voltage supply powering the flash array.

5.3.1.3 Flash reliability specifications.

Table 32. Flash reliability specifications.

Symbol	Description	Min	Typ	Max	Unit	Condition
Tnvmretp10k	Data retention after up to 10 K cycles	10	50	—	years	Program Flash

Table continues on the next page...

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Table 32. Flash reliability specifications....*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
Nnvmcycscr	Sector cycling endurance [1]	10 K	500 K	—	cycles	Program Flash
Tnvmretp1k	Data retention after up to 1 K cycles [2]	20	100	—	years	Program Flash
Tnvmretp100k	Data retention after up to 100 K cycles [2]	5	50	—	years	Program Flash
Nnvmcyc256k	Sector cycling endurance for 256 KB [2][3]	100 K	500 K	—	cycles	Program Flash

[1] Sector cycling endurance represents the number of Program/Erase cycles on a single sector at -40°C ≤ Tj ≤ 125°C.
[2] Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile.
[3] For devices with a single flash block, sectors must be located within the last 256 KB of the flash main memory. For devices with two flash blocks, sectors must be located within the last 256 KB of each flash main memory but must not total more than 256 KB per device.

Note: *Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile.*

5.4 Analog

5.4.1 ADC electrical specifications

5.4.1.1 ADC operating conditions

Table 33. ADC operating conditions

Symbol	Description	Min	Typ	Max	Unit	Condition
VDDAD	Supply voltage	1.71	—	3.6	V	—
VSSAD	Ground voltage	-0.1	0	0.1	V	—
ΔVDD	— [1]	-0.1	0	0.1	V	—
ΔVSS	— [1]	-0.1	0	0.1	V	—
VREFH	Reference Voltage High [2]	0.99	VDDAD	VDDAD	V	—
VREFL	Reference Voltage Low [3]	VSSAD	VSSAD	VSSAD	V	—
VADIN	Input Voltage [3][4][5]	VREFL	—	VREFH	V	—
fADCK	ADC conversion clock frequency	6	—	24	MHz	Low-power mode, PWRSEL=0
fADCK	ADC conversion clock frequency	6	—	64	MHz	Normal Mode, 16b, PWRSEL=1
fADCK	ADC conversion clock frequency	6	—	64	MHz	Normal Mode, 12b , PWRSEL=1
RAS	Analog source resistance (external) [6]	—	—	5	kΩ	—
RADIN	Input Resistance ADC channels 7:0 [7][8]	—	—	1.65	kΩ	VDDAD ≥ 1.71 V

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Table 33. ADC operating conditions...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
RADIN	Input Resistance ADC channels 7:0 [7][8]	—	—	1.525	kΩ	VDDAD ≥ 2.1 V
RADIN	Input Resistance ADC channels 7:0 [7][8]	—	0.925	1.35	kΩ	VDDAD ≥ 2.5 V
CADIN	Input Capacitance	—	1.92	2.4	pF	—

[1] DC potential difference
[2] Minimum VDDAD/VREFH is 2.4 V in high-speed mode (when HS =1)
[3] For devices that do not have a dedicated VREFL and VSS_ANA pins, VREFL and VSS_ANA are tied to VSS internally.
[4] If VREFH is less than VDD_ANA, then voltage inputs greater than VREFH but less than VDD_ANA are allowed but result in a full-scale conversion result
[5] ADC selected inputs and unselected dedicated inputs must not exceed VDD_ANA during an ADC conversion. Unselected muxed inputs may exceed VDD_ANA but must not exceed the IO supply associated with the inputs (VDD) when a conversion is in progress. If an ADC input may exceed these levels, then a minimum of 1 K series resistance must be used between the source and the ADC input pin.
[6] This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible.
[7] There are several types of ADC inputs. To see which channels correspond to which type of ADC inputs, see channel index map in reference manual
[8] If the input come through a mux in the IO pad, add the IO Mux Resistance Adder value to the resistance for the channel type

5.4.1.2 I/O mux resistance table

Table 34. I/O mux resistance table

Symbol	Description	Min	Typ	Max	Unit	Condition
RIOMUX	I/O MUX Resistance	—	—	5.35	kΩ	VDD ≥ 1.71v
RIOMUX	I/O MUX Resistance	—	—	1	kΩ	VDD ≥ 2.1v
RIOMUX	I/O MUX Resistance	—	0.35	0.66	kΩ	VDD ≥ 2.5 v

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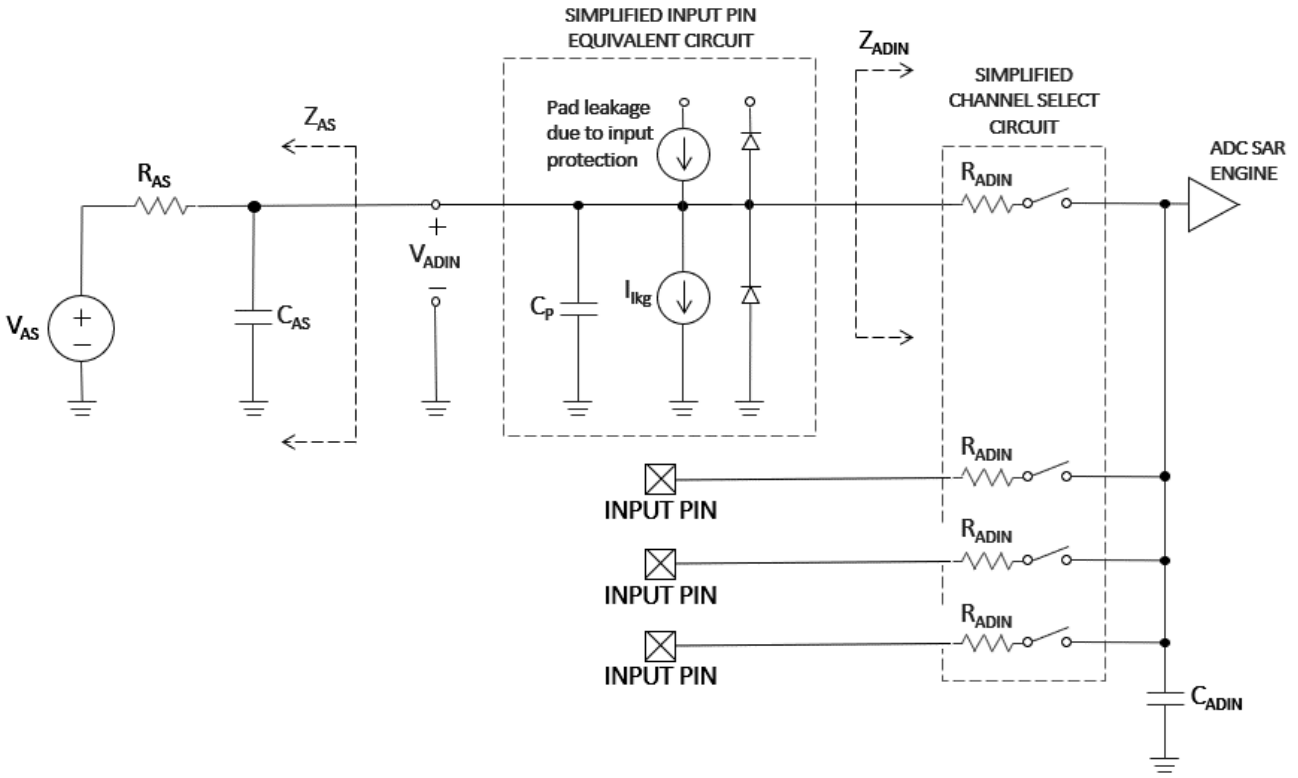


Figure 10. ADC input impedance equivalency diagram

5.4.1.3 ADC electrical characteristics

Note: *Typical values are for reference only and are not tested in production*

Table 35. ADC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Supply current [1]	—	7	—	µA	PWREN=0, Conversions triggered at 10 kS/s
IDDAD	Supply current [1]	—	60	—	µA	PWREN=1, No Conversions
IDDAD	Supply current [1]	—	194	—	µA	Low-power mode, 6 MHz Clock, PWRSEL=0, 16b mode
IDDAD	Supply current [1]	—	251	—	µA	Low-power mode, 24 MHz clock, PWRSEL=0, 16b mode
IDDAD	Supply current [1]	—	658	—	µA	Normal Mode, 64 MHz, PWRSEL=1, 12b mode

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Table 35. ADC electrical characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
IDDAD	Supply current [1]	—	757	—	µA	High Speed Mode, 64 MHz Clock, PWRSEL=1, HS=1, 12b mode
IDDTS	Temp Sensor Supply Current	—	50	—	µA	Temperature Sensor Adder
CSMP	ADC Sample cycles [2]	3.5	—	131.5	cycles	Low-power mode and High speed mode
fconv	ADC conversion rate [3]	—	—	4.0	MS/s	12b mode, (HS=1)
fconv	ADC conversion rate [3]	—	—	3.2	MS/s	16b mode, (HS=1)
tSMP_REQ	Required Sample Time [4]	—	—	—	ns	Use equation based on RAS, RIOMUX, RADIN, CADIN, RAS, CAS, CP and desired accuracy (B)
tSMP	Sample Time [5]	145.8	TSMP_REQ	—	ns	Low-power mode
tSMP	Sample Time [6]	54.7	TSMP_REQ	—	ns	High-speed 16b mode
tSMP	Sample Time [6]	54.7	TSMP_REQ	—	ns	High-speed 12b mode
tSMPINT	Internal channel sample time inputs [7]	2.0	—	—	µs	—
DNL	Differential non-linearity [8][9][10]	—	±0.7	±0.9	LSB	12b mode, N = 12 bits
INL	Integral non-linearity [8][9][10]	—	±0.5	±0.8	LSB	12b mode, N = 12 bits
DNL	Differential non-linearity [8][9][10]	—	±0.5	±0.7	LSB	N = 14 bits, for 16-bit specification, multiply by 4.
INL	Integral non-linearity [8][9][10]	—	±0.5	±0.8	LSB	N = 14 bits, for 16-bit specification, multiply by 4.
ZSE	Zero-scale error (V_ADIN = V_REFL) [9][11]	—	±1	—	LSB	12b mode
FSE	Full-scale error (V_ADIN = V_REFH) [9][11]	—	±2	—	LSB	12b mode
TUE	Total Unadjusted Error [9][11]	—	±3	—	LSB	12b mode
ENOB16	Effective number of bits, 16b Mode, 1 kHz input [9][12]	—	15.0	—	bits	25.2 kS/s (FADCK = 64 MHz, HS =1, AVGS=0111)

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Table 35. ADC electrical characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
ENOB16	Effective number of bits, 16b Mode, 1 kHz input [9][12]	—	13.6	—	bits	200 kS/s (FADCK = 64 MHz, HS=1, AVGS =0100)
ENOB16	Effective number of bits, 16b Mode, 1 kHz input	—	12.7	—	bits	800 kS/s (FADCK = 64 MHz, HS=1, AVGS =0010)
ENOB16	Effective number of bits, 16b Mode, 1 kHz input	—	11.7	—	bits	3.2 MS/s (FADCK = 64 MHz, HS=1, AVGS =0000)
ENOB12	Effective number of bits, 12b Mode, 1 kHz input [9][12]	—	11.5	—	bits	1.0 MS/s (FADCK = 64 MHz, HS =1, AVGS=0010)
ENOB12	Effective number of bits, 12b Mode, 1 kHz input [9][12]	—	11.0	—	bits	4.0 MS/s (FADCK = 64 MHz, HS =1,AVGS=0000)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input [9][12]	—	92.4	—	dB	25.2 kS/s (FADCK=64 MHz, HS=1, AVGS=0111)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input [9][12]	—	84.1	—	dB	200 kS/s (FADCK=64 MHz, HS=1, AVGS=0100)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input [9][12]	—	78.3	—	dB	800 kS/s (FADCK=64MHz, HS=1, AVGS=0010)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input	—	72	—	dB	3.2 MS/s (FADCK=64 MHz, HS=1, AVGS=0000)
SNDR12	Signal-to-noise plus distortion, 12b Mode, 1 kHz input [9][12]	—	71.0	—	dB	1.0 MS/s (FADCK=64 MHz, HS=1, AVGS=0010)
SNDR12	Signal-to-noise plus distortion, 12b Mode, 1 kHz input [9][12]	—	68.0	—	dB	4.0 MS/s (FADCK=64 MHz, HS=1, AVGS=0000)
SFDR	Spurious free dynamic range [9] [12]	—	88.0	—	dB	12b/16b Mode, 1 kHz input, AVGS = 0010
SFDR	Spurious free dynamic range [9] [12]	—	82.0	—	dB	12b/16b Mode, 1 kHz input, AVGS = 0000
tADCSTUP	Start-up time [13]	5	—	—	µs	—
E_TS	Temperature sensor error [14]	—	±1	±3	˚C	Tj = -40 to 105 ˚C
E_TS	Temperature sensor error [14]	—	±2	±4	˚C	Tj = -40 to 125 ˚C

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Table 35. ADC electrical characteristics...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
A	Temp Sensor Slope Constant [15]	—	738.00	—	˚C	—
B	Temp Sensor Offset Constant [15]	—	287.50	—	˚C	—
α	Temp Sensor Bandgap Constant [15]	—	10.06	—	˚C	—

[1] The ADC supply current depends on the ADC conversion clock speed, conversion rate, and power mode. Typical value show is at 6 MHz, 24 MHz, and 64 MHz. For lowest power operation, PWRSEL should be set to 0.
[2] Must meet minimum TSMP requirement
[3] fADCK=64 MHz (HS Mode)
[4] Required sample time is dictated by external components RAS, CAS, internal components RADIN, CADIN, CP, and desired sample accuracy in bits (B). Calculate it with formula: TSMP_REQ = B*ln(2)*[RAS*(CAS+CP+CADIN)+ (RAS + RIOMUX + RADIN)* CADIN(typ). RIOMUX=0 unless the ADC input channel goes through an analog mux in the IO"
[5] Min based on 3.5 cycles
[6] Min based on 3.5 cycles at 64 MHz
[7] Internal channel inputs are those that do not come from external source (temperature sensor, bandgap).
[8] 1 LSB = (VREFH - VREFL)/2^N
[9] All accuracy numbers assume that the ADC is calibrated with VREFH=VDD_ANA and using a high- speed- dedicated input channel. Typical values assume VDD_ANA = 3.0 V, Temp = 25 °C, fADCK = 24 MHz, sample time of 3.5 ADCK cycles (CMDHn[STS]=0h) u nless otherwise stated. Typical values are for reference only, and are not tested in production.
[10] Guaranteed by characterization
[11] 1 LSB = (VREFH - VREFL)/2N (N = 14 bits), for 16- bit specifications, multiply by 4.
[12] Dynamic results assume Fin=1 kHz sinewave, no averaging unless otherwise specified
[13] Delay required if PWREN=0. Set the power-up delay (PUDLY) according to the ADC start-up time if PWREN=0.
[14] The temperature sensor can be calibrated to a +/- 1 % precision after board assembly by using a 3-temperature calibration flow with accurate ± 0.15 % temperature chamber
[15] T(°C) = A*[α(Vbe8 - Vbe1)/(Vbe8 + α(Vbe8 - Vbe1))] - B where Vbe1 is the first value stored to FIFO as a result of the temperature sensor channel conversion, Vbe8 is the second value stored to FIFO as a result of the temperature sensor channel conversion, A is the slope factor, B is the offset factor, α is the bandgap coefficient

Typical values are for reference only and are not tested in production

fADCK = 60 MHz (HS Mode)

Min based on 3.5 cycles at 60 MHz

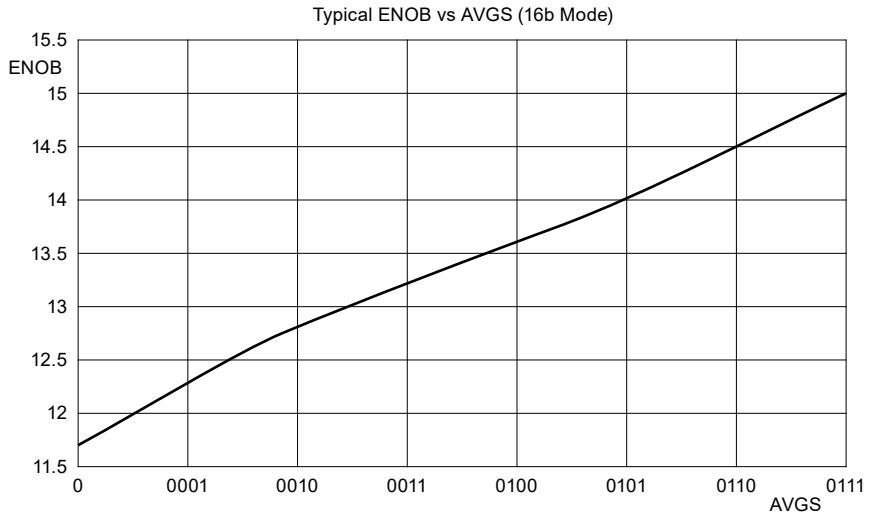


Figure 11. ENOB vs Averaging (16b HS Mode)

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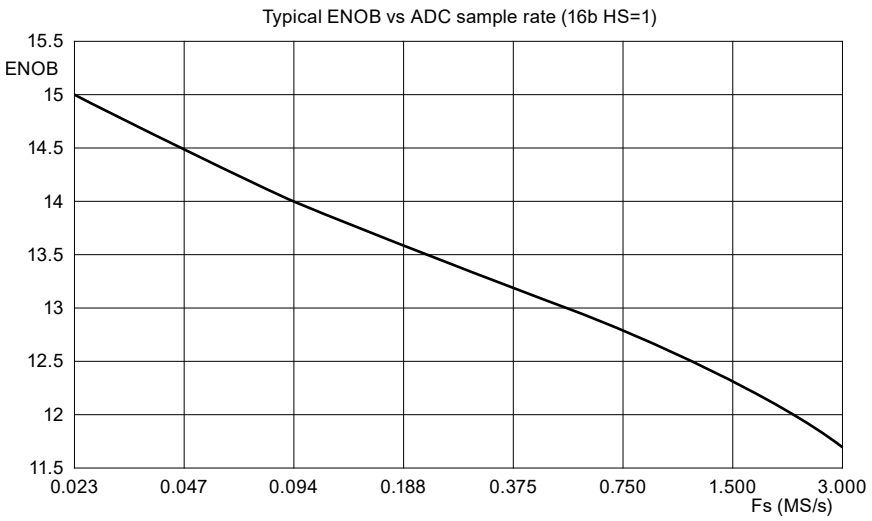


Figure 12. ENOB vs ADC sample rate

5.4.2 12-bit DAC electrical characteristics

5.4.2.1 12-bit DAC operating requirements

Table 36. 12-bit DAC operating requirements

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD_ANA	Supply voltage	1.71	—	3.6	V	—
VDACR	Reference Voltage	0.97	—	VDD_ANA	V	—
CL	Output load capacitance [1]	—	50	100	pF	—
IL	Output load current [2]	-1	—	1	mA	—
DAC_c_rate	DAC conversion rate	—	—	1	MSPS	—

[1] A small load capacitance (50 pF) can improve the bandwidth performance of the DAC.
[2] Sink or source current availability

The DAC reference can be selected to be VDD_ANA or VREFH, keep VDD_ANA be the highest voltage.

5.4.2.2 12-bit DAC operating behaviors

Table 37. 12-bit DAC operating behaviors

Symbol	Description	Min	Typ	Max	Unit	Condition
IDD_DAC	Supply Current	—	300	500	µA	Normal mode
IDD_DAC	Supply Current	—	100	150	µA	Low-power mode
IDD_DAC	Supply Current	—	10	—	nA	Disabled
tDAC	Full-scale settling time (0x100 to 0xF00) [1]	—	2.5	3	µs	Normal mode

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Table 37. 12-bit DAC operating behaviors...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tDAC	Full-scale settling time (0x100 to 0xF00) [1]	—	5	6	µs	Low-power mode
tccDAC	Code-to-code settling time (0xBF8 to 0xC08) [1]	—	0.7	1	µs	—
Vdacoutl	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	—
Vdacouth	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	VDACR-100	—	VDACR	mV	—
INL	Integral non-linearity error [2]	—	—	±3	LSB	—
DNL	Differential non-linearity error [3]	—	—	±1	LSB	—
EOFFSET	Offset error [4]	—	± 0.4	± 0.8	%FSR	—
EG	Gain error [4]	—	± 0.3	± 0.6	%FSR	VDACR < 2.1 V
EG	Gain error [4]	—	± 0.1	± 0.3	%FSR	VDACR > 2.1 V
PSRR	Power supply rejection ratio, VDD_ANA ≥ 2.4 V	—	70	—	dB	—
TCO	Temperature coefficient offset voltage at middle scale [5]	—	—	—	µV/C	—
TEO	Temperature coefficient offset error	—	30	—	µV/C	—
TGE	Temperature coefficient gain error	—	10	—	PPM/C	—
ROP	Output resistance (load = 10 kΩ)	—	200	—	Ω	—
SR	Slew rate 100 h ->F00 h or F00 h ->100 h	—	3.6	—	V/µs	—
SR	Slew rate 100 h ->F00 h or F00 h ->100 h	—	0.5	—	V/µs	—
tPU	Power-up time	—	2.5	—	µs	—

[1] Settling within ±1 LSB measured with a 47 pF load.
[2] The INL is measured for 0 + 100 mV to VDACR −100 mV
[3] The DNL is measured for 0 + 100 mV to VDACR −100 mV
[4] Calculated by a best fit curve from VSS_ANA + 100 mV to VDACR − 100 mV
[5] VDD_ANA = 3.0 V, reference select set for VDD_ANA (DACx_CO:DACRFS = 1), high- power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device.

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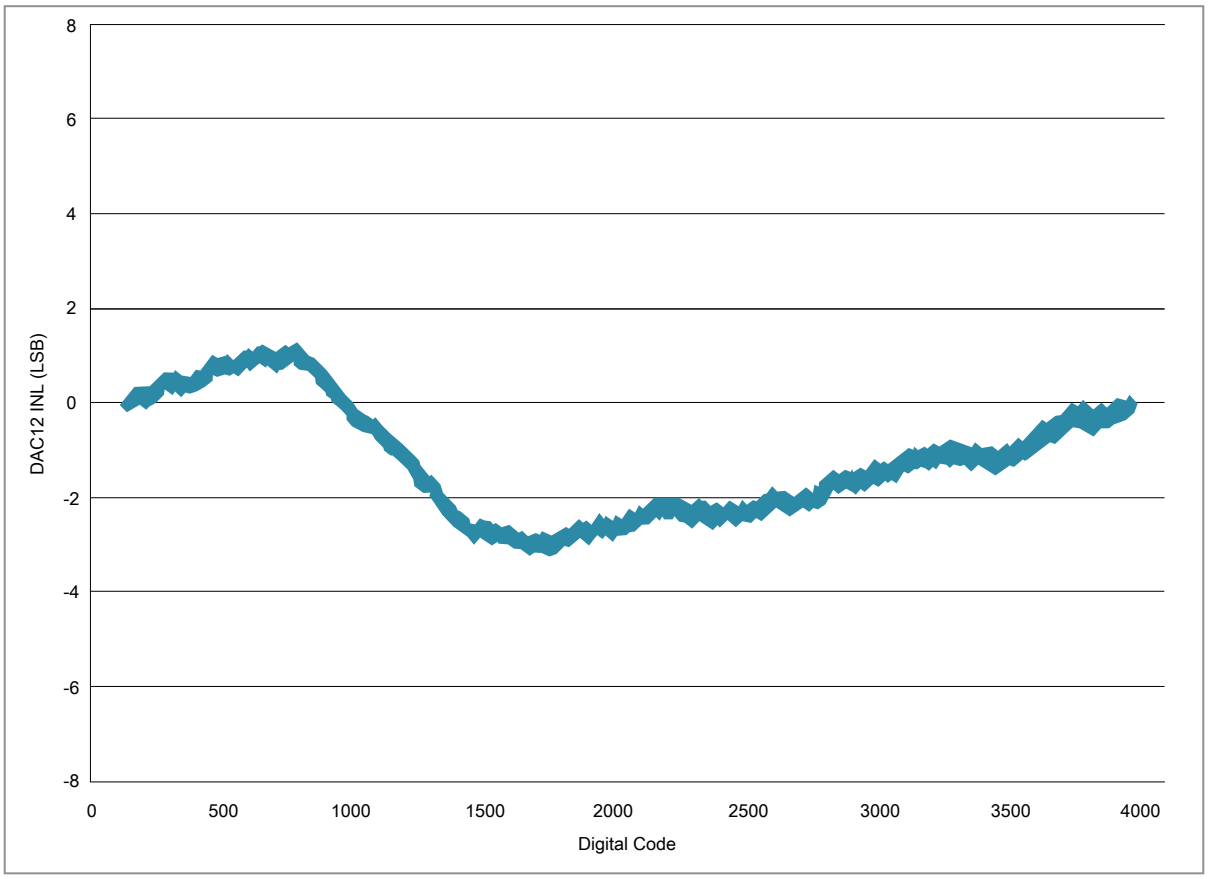


Figure 13. Typical INL error vs. digital code

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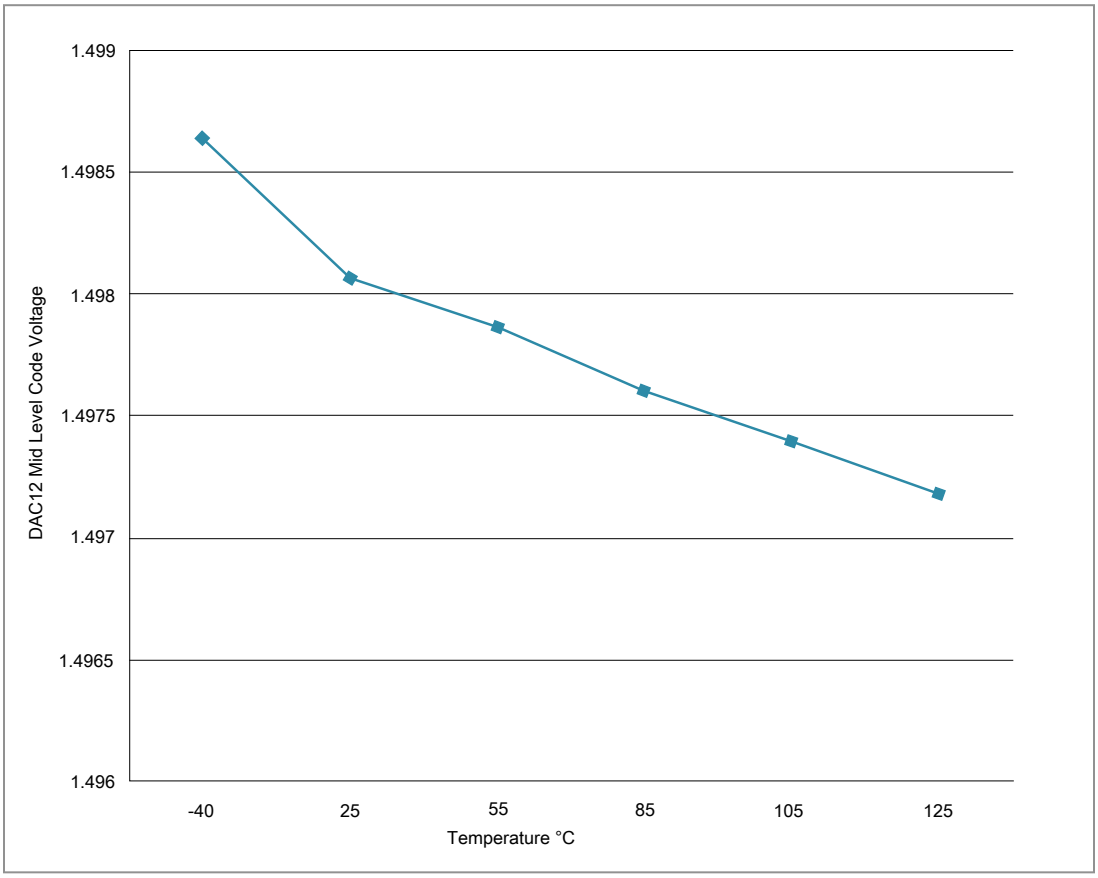


Figure 14. Offset at half scale vs. temperature

5.4.3 Comparator and 8-bit DAC electrical specifications

Table 38. Comparator and 8-bit DAC electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	Supply voltage	1.71	—	3.6	V	—
VREFH	8-bit DAC reference voltage high	0.97	—	VDD	V	—
IDD_CMP	Supply current	—	200	—	µA	High speed mode (EN=1, HPMD=1)
IDD_CMP	Supply current	—	10	—	µA	Normal mode (EN=1, HPMD=0, NPMD=0)
IDD_CMP	Supply current	—	400	—	nA	Low-power mode (EN=1, HPMD=0, NPMD=1)
VAIN	Analog input voltage	VSS	—	VDD	V	—
VAIO	Analog input offset voltage	—	—	20	mV	High speed mode

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Table 38. Comparator and 8-bit DAC electrical specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
VAIO	Analog input offset voltage	—	—	20	mV	Normal mode
VAIO	Analog input offset voltage	—	—	40	mV	Low-power mode
VH	Analog comparator hysteresis [1]	—	0	—	mV	CR0[HYSTCTR] = 00
VH	Analog comparator hysteresis [1]	—	10	—	mV	CR0[HYSTCTR] = 01
VH	Analog comparator hysteresis [1]	—	20	—	mV	CR0[HYSTCTR] = 10
VH	Analog comparator hysteresis [1]	—	30	—	mV	CR0[HYSTCTR] = 11
VCMPOh	Output high	VDD - 0.2	—	—	V	—
VCMPOl	Output low	—	—	0.2	V	—
tD	Propagation delay [2]	—	—	25	ns	High speed mode, 100 mV overdrive, power > 1.71V
tD	Propagation delay [2]	—	—	50	ns	High speed mode, 30 mV overdrive, power > 1.71V
tD	Propagation delay [2]	—	—	600	ns	Normal mode, 30 mV overdrive, power > 1.71V
tD	Propagation delay [2]	—	—	5	µs	Low-power mode, 30 mV overdrive, power > 1.71V
tinit	Analog comparator initialization delay [3]	—	—	40	µs	—
IDAC8b	8-bit DAC current adder (enabled)	—	10	—	µA	High power mode (EN=1, PMODE=1)
IDAC8b	8-bit DAC current consumption	—	1	—	µA	Low power mode (EN=1, PMODE=0)
INL	8-bit DAC integral non-linearity [4]	-1	—	+1.0	LSB	Low/High power mode, supply power > 1.71V
DNL	8-bit DAC differential non-linearity	-1	—	+1.0	LSB	Low/High power mode, power > 1.71V

[1] Typical hysteresis is measured with input voltage range limited to 0.6 to VDD_ANA–0.6 V.
[2] Overdrive does not include input offset voltage or hysteresis. The propagation delay is defined as the time delay between the change of the voltage on input pin and the output change of the comparator analog part
[3] Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
[4] 1 LSB = Vreference/256

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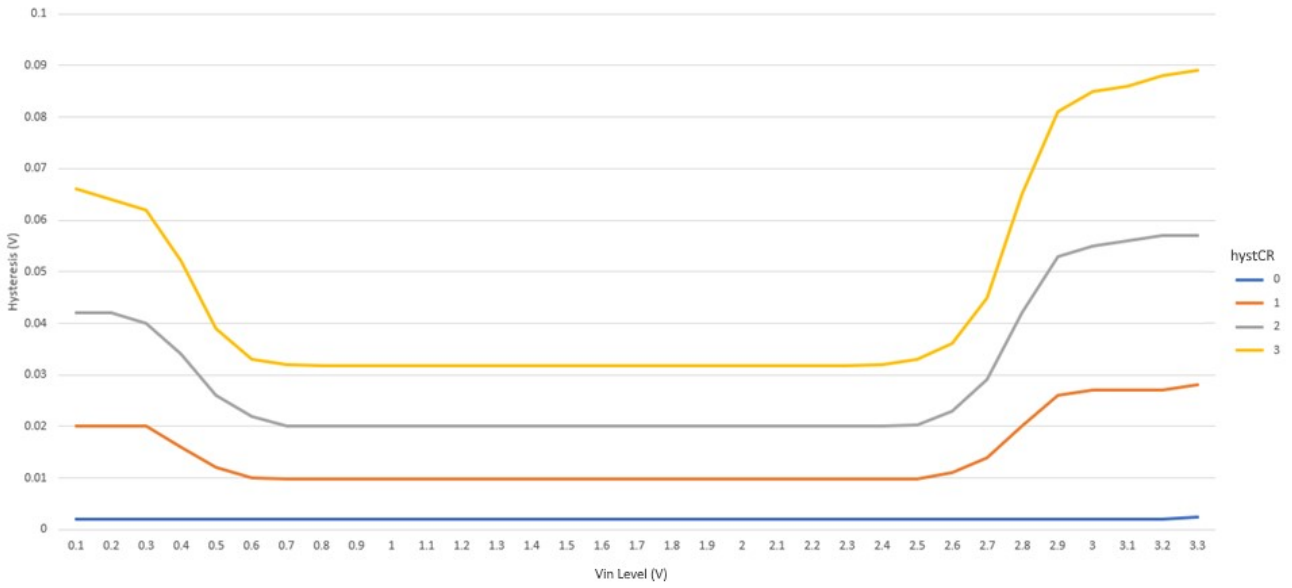


Figure 15. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 1)

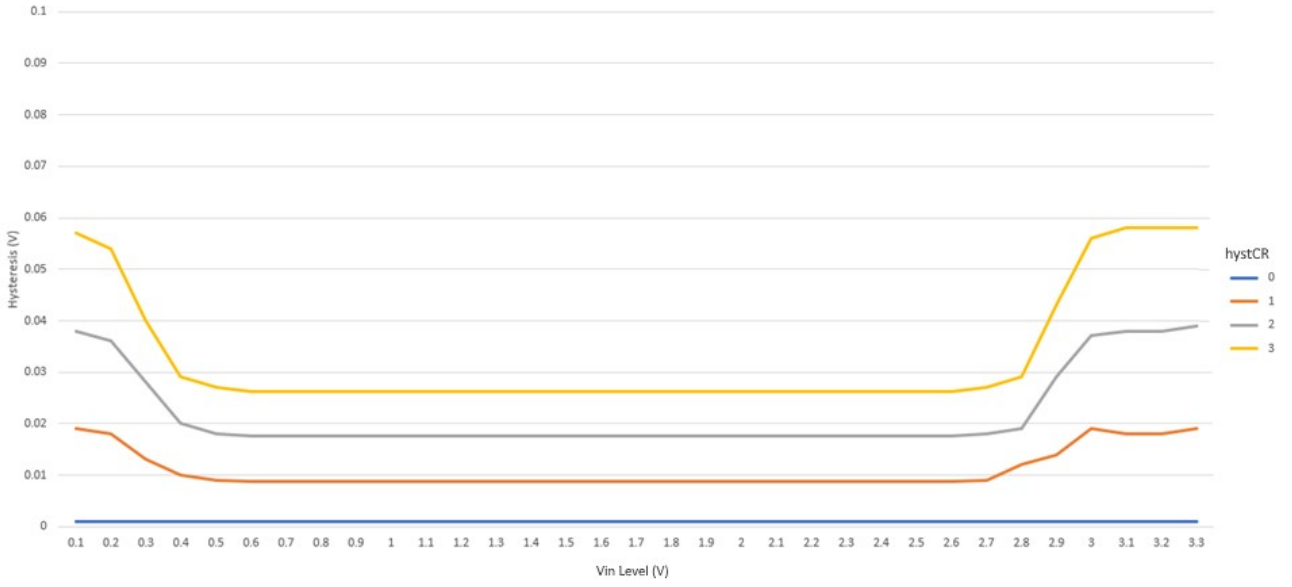


Figure 16. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 0)

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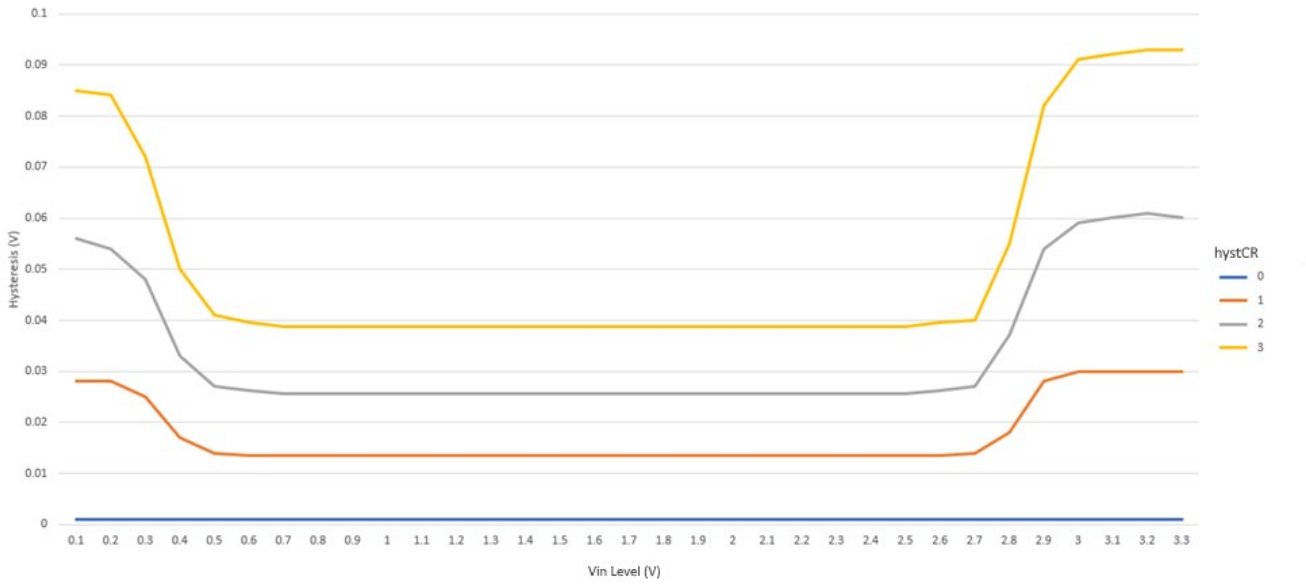


Figure 17. Typical hysteresis vs Vin level (VDD =3.3 V, HPMD = 0, NPMD = 1)

5.4.4 OpAmp electrical specifications

Table 39. OpAmp electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
TJ	Operation temperature	-40	25	125	°C	—
Vvdda	Analog supply voltage	1.71	3	3.6	V	—
Vvdd	Digital supply voltage	0.9	1.1	1.21	V	—

Table 40. OpAmp electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
Ivdda	Analog supply current	—	500	—	µA	—
Cin	Input capacitance	—	—	5	pF	—
Cload	Load capacitance	—	—	20	pF	—
Rload	Load resistance	3	—	20	KΩ	—
Vcm	Input common mode voltage range	0	—	Vvdda-1	V	—
Vout	Output voltage range	0.15	—	Vvdda - 0.15	V	—
Ishuntdown_3v	Leakage current for vdda_3v pin	—	1	80	nA	When Vvdda = 3V

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Table 40. OpAmp electrical specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
Vos	Input offset voltage	-7	0	7	mV	—
CMRR	Input common mode rejection ratio	—	80	—	dB	—
PSRR	Power supply rejection ratio	—	80	—	dB	—
UGB	Unity gain bandwidth	—	8	—	MHz	CC config=2'b00, gain=2
UGB	Unity gain bandwidth	—	16	—	MHz	CC config=2'b01, gain=4
UGB	Unity gain bandwidth	—	32	—	MHz	CC config=2'b10, gain=8
UGB	Unity gain bandwidth	—	64	—	MHz	CC config=2'b11, gain=16
Av	DC open loop voltage gain	-	95	-	dB	—
PM	Phase marge	-	60	-	deg	—
tsettle	Settling time	-	450	-	ns	—
SR	Slew rate	-	10	-	V/us	—
Vn	Voltage noise density @1KHz	—	150	—	nV/ sqrtHz	Gain = 1
Zout	Closed-loop output impedance	—	1.703	—	Ω	cc config=2'b00, f = 200KHz
Zout	Closed-loop output impedance	—	14.72	—	Ω	cc config=2'b01, f = 200KHz
Zout	Closed-loop output impedance	—	8.514	—	Ω	cc config=2'b00, f = 1MHz
Zout	Closed-loop output impedance	—	73.47	—	Ω	cc config=2'b01, f = 1MHz

5.5 Timers

See General switching specifications.

5.6 Communication Interfaces

5.6.1 LPUART

See General switching specifications.

5.6.2 LPSPI switching specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with controller and peripheral operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes.

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5.6.2.1 LPSPI controller mode timing

Table 41. LPSPI controller mode timing

Symbol	Description	Min	Typ	Max	Unit	Condition
LP1	Frequency of operation [1]	—	—	—	MHz	—
LP1	LPSPI0 ~ LPSPI1 medium speed pad [2]	—	—	50	MHz	Controller in OD mode
LP1	LPSPI0 ~ LPSPI1 slow speed pad [2]	—	—	25	MHz	Controller in OD mode
LP1	LPSPI0 ~ LPSPI1 medium speed pad [2]	—	—	25	MHz	Controller in MD mode
LP1	LPSPI0 ~ LPSPI1 slow speed pad [2]	—	—	25	MHz	Controller in MD mode
LP2	SPSCK period	1000/LP1	—	—	ns	—
LP3	Enable lead time [3]	1/2	—	—	tperiph	—
LP4	Enable lag time [3]	1/2	—	—	tperiph	—
LP5	Clock (SPSCK) high or low time	tSCK/2-3	—	tSCK/2	ns	—
LP6	Data setup time (inputs)	—	—	—	ns	—
LP6	LPSPI0 ~ LPSPI1 medium speed pad [2]	—	—	4.2	ns	Controller in OD mode
LP6	LPSPI0 ~ LPSPI1 slow speed pad [2]	—	—	4.4	ns	Controller in OD mode
LP6	LPSPI0 ~ LPSPI1 medium speed pad [2]	—	—	5.4	ns	Controller in MD mode
LP6	LPSPI0 ~ LPSPI1 slow speed pad [2]	—	—	5.4	ns	Controller in MD mode
LP7	Data hold time (inputs)	—	—	—	ns	—
LP7	LPSPI0 ~ LPSPI1 medium speed pad [2]	0	—	—	ns	Controller in OD mode
LP7	LPSPI0 ~ LPSPI1 slow speed pad [2]	0	—	—	ns	Controller in OD mode
LP7	LPSPI0 ~ LPSPI1 medium speed pad [2]	0	—	—	ns	Controller in MD mode
LP7	LPSPI0 ~ LPSPI1 slow speed pad [2]	0	—	—	ns	Controller in MD mode
LP8	Data valid (after SPSCK edge)	—	—	—	ns	—
LP8	LPSPI0 ~ LPSPI1 medium speed pad [2]	—	—	6.4	ns	Controller in OD mode
LP8	LPSPI0 ~ LPSPI1 slow speed pad [2]	—	—	12.8	ns	Controller in OD mode

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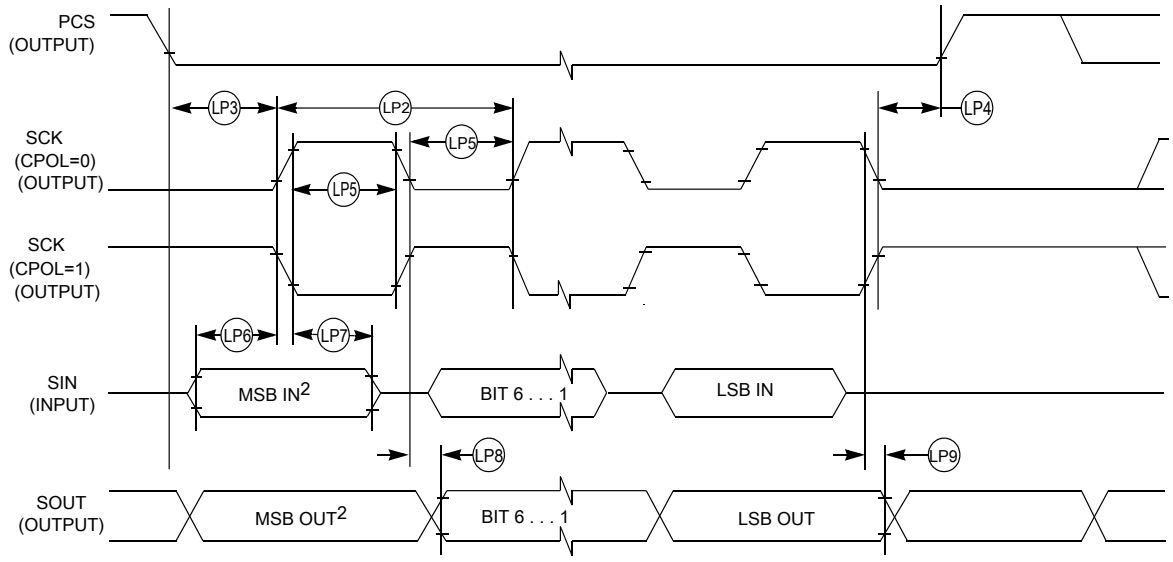
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Table 41. LPSPI controller mode timing*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
LP8	LPSPI0 ~ LPSPI1 medium speed pad [2]	—	—	13.6	ns	Controller in MD mode
LP8	LPSPI0 ~ LPSPI1 slow speed pad [2]	—	—	13.6	ns	Controller in MD mode
LP9	Data hold time (outputs)	—	—	—	ns	—
LP9	LPSPI0 ~ LPSPI1 medium speed pad [2]	-1	—	—	ns	Controller in OD mode
LP9	LPSPI0 ~ LPSPI1 slow speed pad [2]	-1	—	—	ns	Controller in OD mode
LP9	LPSPI0 ~ LPSPI1 medium speed pad [2]	-1	—	—	ns	Controller in MD mode
LP9	LPSPI0 ~ LPSPI1 slow speed pad [2]	-1	—	—	ns	Controller in MD mode

[1] The frequency of operation is also limited to a minimum of fperiph/2048 and a max of fperiph/2, where fperiph is the LPSPI peripheral functional clock.
[2] OD mode is MCU at Over drive mode, MD mode is MCU at Middle drive mode.
[3] tperiph = 1/fperiph

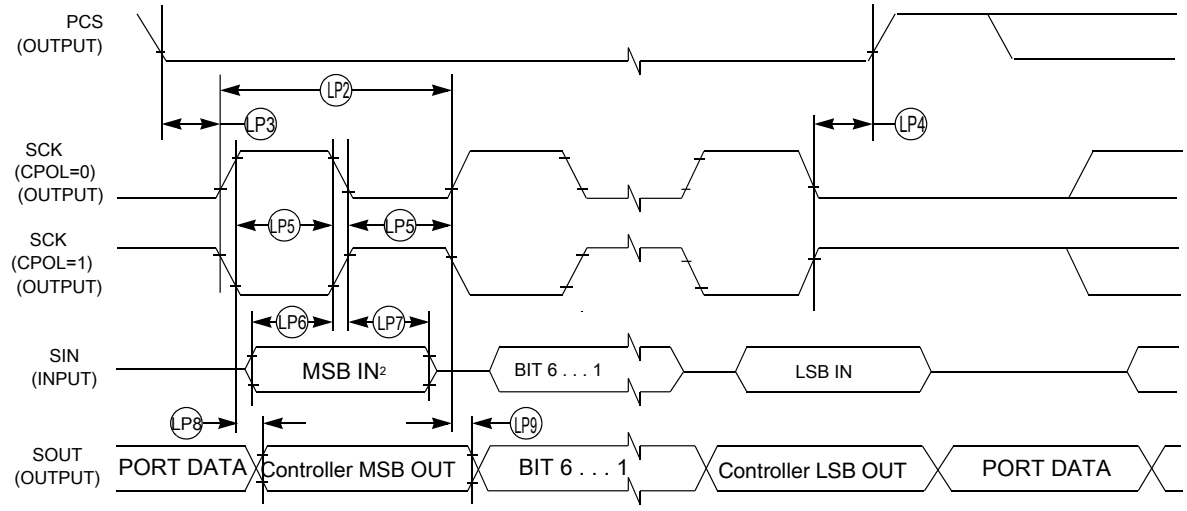


1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. LPSPI controller mode timing (CPHA = 0)

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1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 19. LPSPI controller mode timing (CPHA = 1)

5.6.2.2 LPSPI peripheral mode timing

Table 42. LPSPI peripheral mode timing

Symbol	Description	Min	Typ	Max	Unit	Condition
LP1	Frequency of operation in OD mode [1]	—	—	—	—	—
LP1	lpspi0~lpspi1 medium speed pad [1]	—	—	25	MHz	Peripheral Tx in OD mode
LP1	lpspi0~lpspi1 slow speed pad [1]	—	—	12.5	MHz	Peripheral Tx in OD mode
LP1	lpspi0~lpspi1 medium speed pad	—	—	50	MHz	Peripheral Rx in OD mode
LP1	lpspi0~lpspi1 slow speed pad	—	—	25	MHz	Peripheral Rx in OD mode
LP1	lpspi0~lpspi1 medium speed pad	—	—	12	MHz	Peripheral Tx in MD mode
LP1	lpspi0~lpspi1 slow speed pad	—	—	12	MHz	Peripheral Tx in MD mode
LP1	lpspi0~lpspi1 medium speed pad	—	—	12	MHz	Peripheral Rx in MD mode
LP1	lpspi0~lpspi1 slow speed pad	—	—	12	MHz	Peripheral Rx in MD mode
LP2	SPSCK period	4 x tperiph	—	2048 x tperiph	ns	—
LP3	Enable lead time [2]	1	—	—	tperiph	—

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Table 42. LPSPI peripheral mode timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
LP4	Enable lag time [2]	1	—	—	tperiph	—
LP5	Clock (SPSCK) high or low time	tSPSCK/2 - 5	—	tSPSCK/2	ns	—
LP6	Data setup time (inputs)	—	—	—	ns	—
LP6	lpspi0~lpspi1 medium speed pad	—	—	3.6	ns	Peripheral Rx in OD mode
LP6	lpspi0~lpspi1 slow speed pad	—	—	7.2	ns	Peripheral Rx in OD mode
LP6	lpspi0~lpspi1 medium speed pad	—	—	12.8	ns	Peripheral Rx in MD mode
LP6	lpspi0~lpspi1 slow speed pad	—	—	12.8	ns	Peripheral Rx in MD mode
LP7	Data hold time (inputs)	—	—	—	ns	—
LP7	lpspi0~lpspi1 medium speed pad	0	—	—	ns	Peripheral Rx in OD mode
LP7	lpspi0~lpspi1 slow speed pad	0	—	—	ns	Peripheral Rx in OD mode
LP7	lpspi0~lpspi1 medium speed pad	0	—	—	ns	Peripheral Rx in MD mode
LP7	lpspi0~lpspi1 slow speed pad	0	—	—	ns	Peripheral Rx in MD mode
LP8	Peripheral access time [2][3]	—	—	tperiph	ns	—
LP9	Peripheral MISO disable time [2] [4]	—	—	tperiph	ns	—
LP10	Data valid (after SPSCK edge)	—	—	—	ns	—
LP10	lpspi0~lpspi1 medium speed pad	—	—	15.6	ns	Peripheral Tx in OD mode
LP10	lpspi0~lpspi1 slow speed pad	—	—	31.2	—	Peripheral Tx in OD mode
LP10	lpspi0~lpspi1 medium speed pad	—	—	29.2	ns	Peripheral Tx in MD mode
LP10	lpspi0~lpspi1 slow speed pad	—	—	29.2	ns	Peripheral Tx in MD mode
LP11	Data hold time (outputs)	—	—	—	ns	—
LP11	lpspi0~lpspi1 medium speed pad	2	—	—	ns	Peripheral Tx in OD mode
LP11	lpspi0~lpspi1 slow speed pad	2	—	—	ns	Peripheral Tx in OD mode

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Table 42. LPSPI peripheral mode timing*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
LP11	lpspi0~lpspi1 medium speed pad	2	—	—	ns	Peripheral Tx in MD mode
LP11	lpspi0~lpspi1 slow speed pad	2	—	—	ns	Peripheral Tx in MD mode

[1] The frequency of operation is also limited to a minimum of fperiph/2048 and a max of fperiph/4, where fperiph is the LPSPI peripheral functional clock.
[2] tperiph = 1/fperiph
[3] Time to data active from high-impedance state
[4] Hold time to high-impedance state

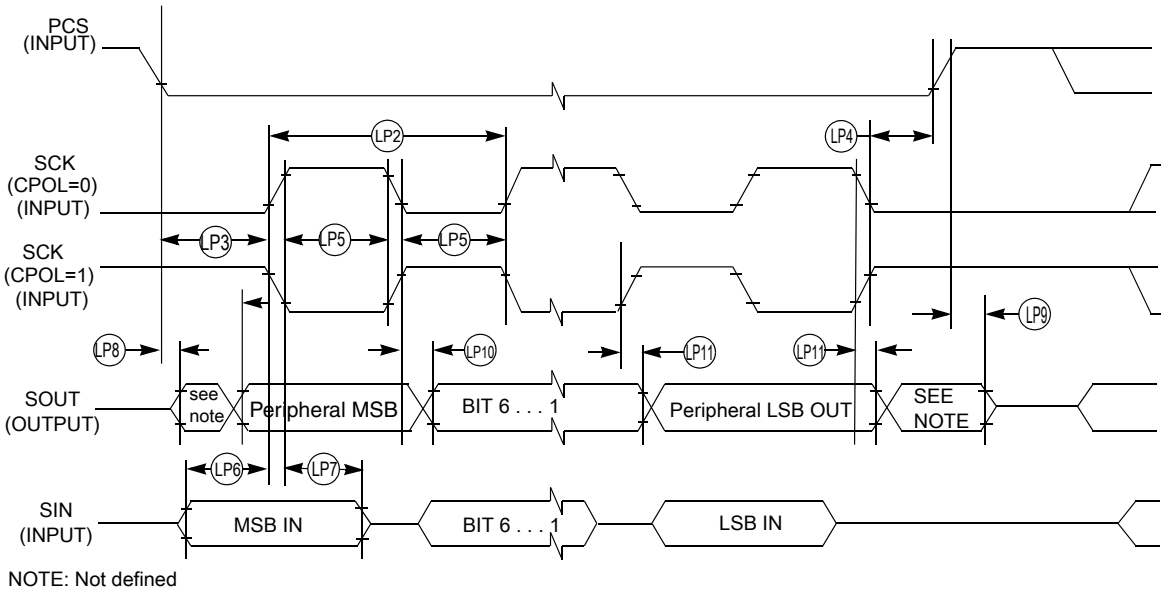


Figure 20. LPSPI peripheral mode timing (CPHA = 0)

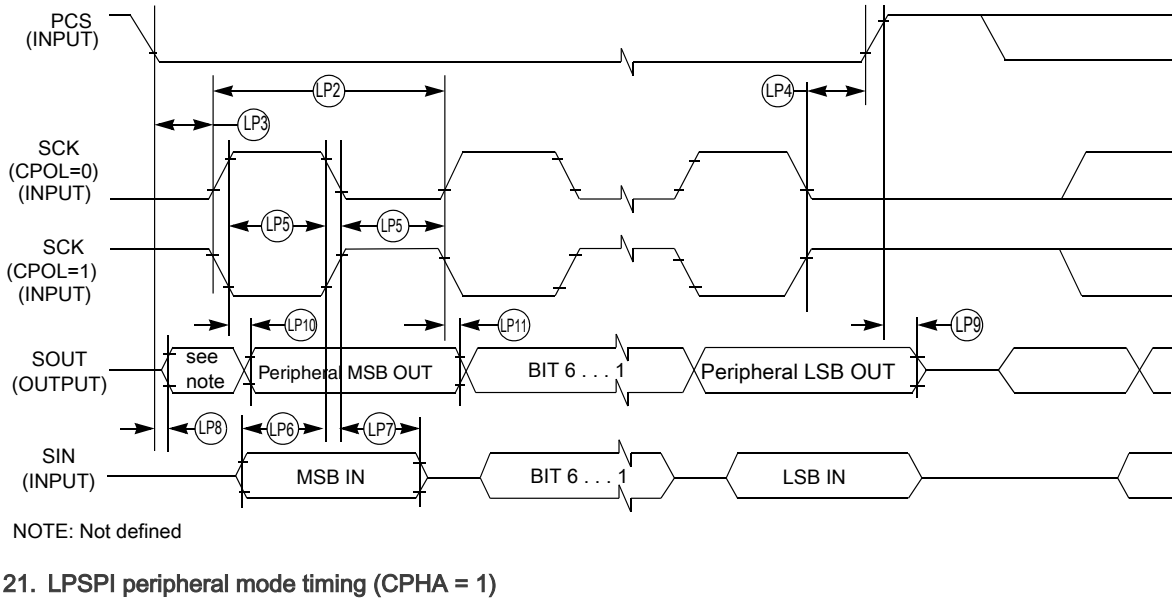


Figure 21. LPSPI peripheral mode timing (CPHA = 1)

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5.6.3 LPI2C timing

Table 43. LPI2C timing

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency in standard mode	0	—	100	kHz	—
fSCL	SCL Clock Frequency in fast mode	0	—	400	kHz	—
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated in standard mode	4	—	—	µs	—
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated in fast mode	0.6	—	—	µs	—
tLOW	LOW period of the SCL clock in standard mode	4.7	—	—	µs	—
tLOW	LOW period of the SCL clock in fast mode	1.25	—	—	µs	—
tHIGH	HIGH period of the SCL clock in standard mode	4	—	—	µs	—
tHIGH	HIGH period of the SCL clock in fast mode	0.6	—	—	µs	—
tSU; STA	Set-up time for a repeated START condition in standard mode	4.7	—	—	µs	—
tSU; STA	Set-up time for a repeated START condition in fast mode	0.6	—	—	µs	—
tHD; DAT	Data hold time for I2C bus devices in standard mode [1][2]	0	—	3.45	µs	—
tHD; DAT	Data hold time for I2C bus devices in fast mode [1][3]	0	—	0.9	µs	—
tSU; DAT	Data set-up time in standard mode [4]	250	—	—	ns	—
tSU; DAT	Data set-up time in fast mode [2][5]	100	—	—	ns	—
tr	Rise time of SDA and SCL signals in standard mode [6]	—	—	1000	ns	—
tr	Rise time of SDA and SCL signals in fast mode [6]	20 +0.1Cb	—	300	ns	—
tf	Fall time of SDA and SCL signals in standard mode [5]	—	—	300	ns	—

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Table 43. LPI2C timing*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tf	Fall time of SDA and SCL signals in fast mode [5]	20 +0.1Cb	—	300	ns	—
tSU; STO	Set-up time for STOP condition in standard mode	4	—	—	µs	—
tSU; STO	Set-up time for STOP condition in fast mode	0.6	—	—	µs	—
tBUF	Bus free time between STOP and START condition in standard mode	4.7	—	—	µs	—
tBUF	Bus free time between STOP and START condition in fast mode	1.3	—	—	µs	—
tSP	Pulse width of spikes that must be suppressed by the input filter in standard mode	N/A	—	N/A	ns	—
tSP	Pulse width of spikes that must be suppressed by the input filter in fast mode	0	—	50	ns	—

[1] The controller mode I2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no targets acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
[2] The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal
[3] Input signal Slew = 10 ns and Output Load = 50 pF
[4] Set-up time in target-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
[5] A Fast mode I2C bus device can be used in a Standard mode I2C bus system, but the requirement tSU; DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line trmax + tSU; DAT = 1000 + 250 = 1250 ns (according to the Standard mode I2C bus specification) before the SCL line is released.
[6] Cb = total capacitance of the one bus line in pF.

5.6.4 I2C 1 Mbps timing

Table 44. I2C 1 Mbps timing

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency	0	—	1	MHz	—
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26	—	—	µs	—
tLOW	LOW period of the SCL clock	0.5	—	—	µs	—
tHIGH	HIGH period of the SCL clock	0.26	—	—	µs	—
tSU; STA	Set-up time for a repeated START condition	0.26	—	—	µs	—
tHD; DAT	Data hold time for I2C bus devices	0	—	—	µs	—
tSU; DAT	Data set-up time	50	—	—	ns	—

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Table 44. I2C 1 Mbps timing*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tr	Rise time of SDA and SCL signals [1]	20 +0.1Cb	—	120	ns	—
tf	Fall time of SDA and SCL signals [1]	20 +0.1Cb	—	120	ns	—
tSU; STO	Set-up time for STOP condition	0.26	—	—	µs	—
tBUF	Bus free time between STOP and START condition	0.5	—	—	µs	—
tSP	Pulse width of spikes that must be suppressed by the input filter	0	—	50	ns	—

[1] Cb = total capacitance of the one bus line in pF for maximum value

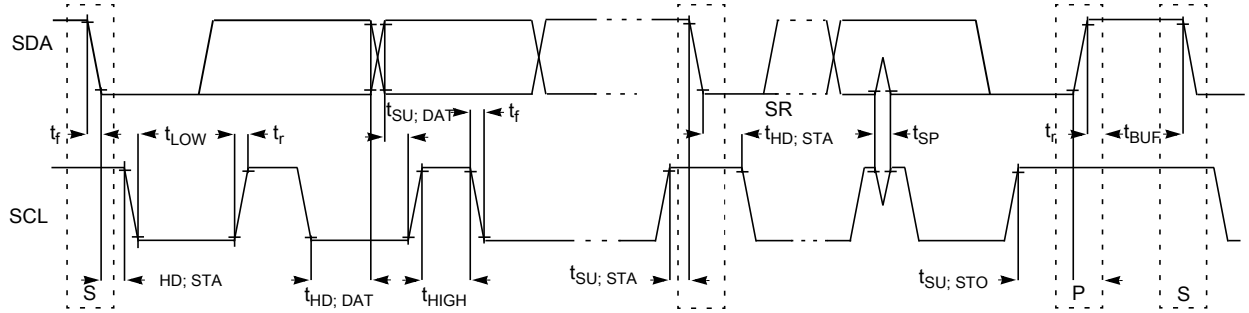


Figure 22. Timing definition for devices on the I2C bus

5.6.5 I2C HS mode timing

Table 45. I2C HS mode timing

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency	0	—	3.4	MHz	—
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26	—	—	µs	—
tLOW	LOW period of the SCL clock	0.5	—	—	µs	—
tHIGH	High period of the SCL clock	0.26	—	—	µs	—
tSU; STA	Set-up time for a repeated START condition	0.26	—	—	µs	—
tHD; DAT	Data hold time for I2C bus devices [1]	0	—	—	µs	—
tSU; DAT	Data setup time	34	—	—	ns	—
tr	Rise time of SDA and SCL signals [2]	20 +0.1Cb	—	120	ns	—

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Table 45. I2C HS mode timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tf	Fall time of SDA and SCL signals [2]	20 +0.1Cb	—	120	ns	—
tSU; STO	Setup time for STOP condition	0.26	—	—	µs	—
tBUF	Bus free time between STOP and START condition	0.5	—	—	µs	—
tSP	Pulse width of spikes that must be suppressed by the input filter	0	—	50	ns	—

[1] A device must internally provide a data hold time to bridge the undefined part between VIH and VIL of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time in maximum value.
[2] Cb = total capacitance of the one bus line in pF. The typical Cb value is 20 pF

5.6.6 I3C Push-Pull Timing Parameters for SDR Mode

I3C interface is not supported on GPIO-Standard-plus pad type for 5 V operation. Measurements are with maximum output load of 30 pf, input transition of 1 ns. GPIO-Standard-plus pad configured with DSE = 1'b1 and GPIO-Medium pad with DSE = 1'b1 and SRE = 1'b1. SCL, SDA and PUR combination should be of same pad type. For e.g. I3C medium Data Pads to be used with I3C Medium Clock and PUR Pads Only. I3C Standard plus Data Pads to be used with I3C standard plus Clock and PUR pads only.

Table 46. I3C Push-Pull Timing Parameters for SDR Mode

Symbol	Description	Min	Typ	Max	Measurement Timing	Unit	Condition
fSCL	SCL Clock Frequency	0.01	12.5	12.9	—	MHz	FSCL = 1 / (tDIG_L + tDIG_H)
tDIG_L	SCL Clock Low Period [1]	32	—	—	—	ns	—
tDIG_H	SCL Clock High Period [2]	32	—	—	—	ns	—
tSCO	Clock in to Data Out for Target [3][4]	—	—	12	21.51[5]	ns	in MD mode
					18.09[5]	ns	in OD mode
tCR	SCL Clock Rise Time [6]	—	—	150e06 * 1 / fSCL (capped at 60)	—	ns	—
tCF	SCL Clock Fall Time						
tHD_PP	SDA Signal Data Hold in Push-Pull Mode, Target [7]	0	—	—	—	—	Applicable for target and controller loopback modes
tSU_PP	SDA Signal Data Setup in Push-Pull Mode	3	—	—	—	ns	Applicable for target and controller loopback modes

[1] As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., tCF + 3 for falling edge clocks, and tCR + 3 for rising edge clocks.
[2] tDIG_L and tDIG_H are the clock Low and High periods as seen at the receiver end of the I3C Bus using VIL and VIH (see Figure 30)
[3] Devices with more than 12ns of tSCO delay shall set the limitation bit in the BCR, and shall support the GETMXDS CCC to allow the Controller to read this value and adjust computations accordingly. For purposes of system design and test conformance, this parameter should be considered together with pad delay, bus capacitance, propagation delay, and clock triggering points.

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[4] Pad delay based on 90 Ω / 4 mA driver and 50 pF load. Note that Controller may be a Target in a multi-Controller system, and thus shall also adhere to this requirement
[5] Guaranteed by design
[6] The clock maximum rise/fall time is capped at 60 ns. For lower frequency rise and fall the maximum value is limited at 60 ns, and is not dependent upon the clock frequency.
[7] tHD_PP is a Hold time parameter for Push-Pull Mode that has a different value for Controller mode vs. Target mode. In SDR Mode the Hold time parameter is referred to as tHD_SDR.

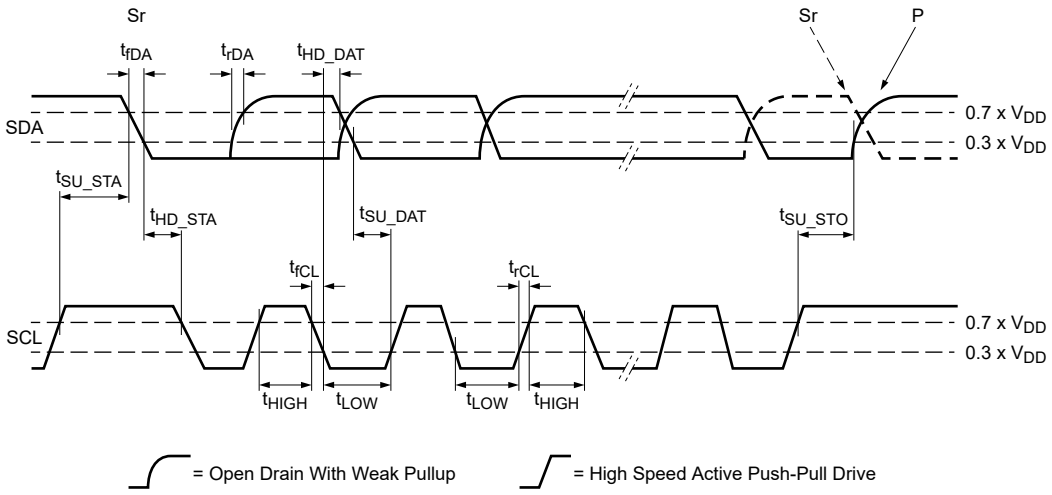


Figure 23. Legacy mode timing

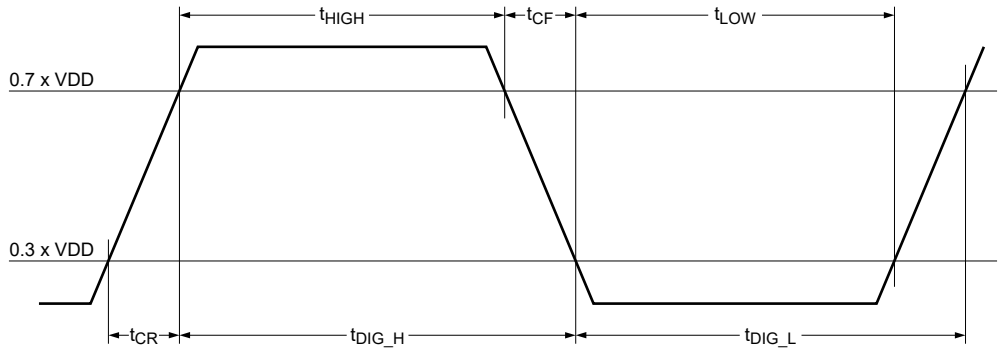


Figure 24. tDIG_H and tDIG_L

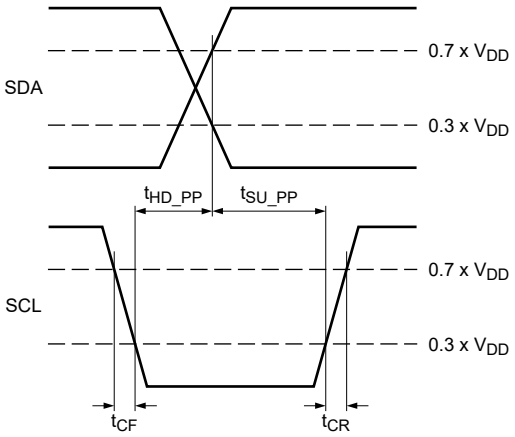


Figure 25. Controller out timing

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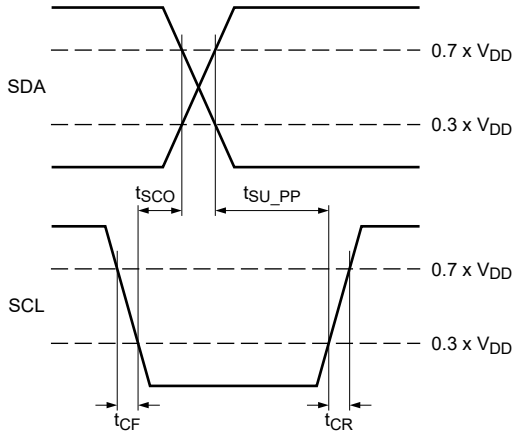


Figure 26. Target out timing

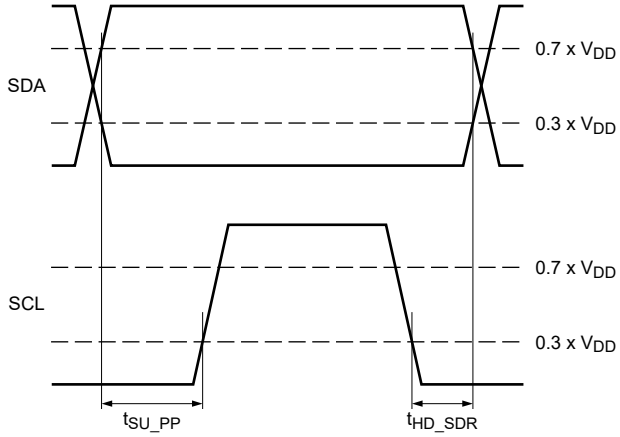


Figure 27. Controller SDR timing

5.6.7 USB Full-speed device electrical specifications

This section describes the USB0 port Full Speed/Low Speed transceiver. The USB0 (FS/LS Transceiver) meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 Specification with the amendments below.

- USB ENGINEERING CHANGE NOTICE
  - Title: 5 V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0

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This SoC does not have a dedicated pin to monitor the state of the USB VBUS signal. Please refer to the USBFS chapter in the Reference Manual for methods which can be used for VBUS Session_Valid detection with either a P4-12/ALT1 pin using an external resistive divider.

5.6.8 Flexible I/O controller (FLEXIO) electrical specifications

The following table shows FlexIO timing specifications.

Table 47. Flexible I/O controller (FLEXIO) electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
tODS	Output delay skew between any two FlexIO_Dx pins configured as outputs that toggle on same internal clock cycle	0	—	8	ns	—
tIDS	Input delay skew between any two FlexIO_Dx pins configured as inputs that are sampled on the same internal clock cycle	0	—	8	ns	—

5.6.9 FlexCAN

See General switching specifications.

5.7 Human Machine Interface (HMI) modules

5.7.1 General Purpose Input/Output (GPIO)

See General switching specifications.

5.7.2 Segment LCD electrical specification

Table 48. Segment LCD electrical specification

Symbol	Description	Min	Typ	Max	Unit	Condition
TJ	Operation temperature	-40	27	115	°C	—
Vvdd_3v	Analog supply voltage	2.7	3	3.3	V	—
Vvdd_lv	Digital supply voltage	0.81	1.1	1.21	V	—
Cbypass	Bypass capacitor for Vlcd_vll2_3v and Vlcd_vll1_3v	80	100	120	nF	—
Rser	Resistance in series with bypass capacitor	—	—	100	Ω	—
Cglass	LCD glass capacitor	—	—	8	nF	—
Fclk	Clock signal	—	16	—	kHz	—
Ivdd_3v	Current consumption at room temp	—	6	—	µA	normal mode
Ivdd_3v	Current consumption at room temp	—	1	—	µA	S&H mode

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Table 48. Segment LCD electrical specification*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
Ishuntdown_3v	Leakage current for vdd_3v pin	—	1	—	nA	Disabled
Vlcd_vll3_3v	LCD bias voltage level 3	—	1	—	Vvdd_3v	—
Vlcd_vll2_3v	LCD bias voltage level 2	—	0.67	—	Vvdd_3v	—
Vlcd_vll1_3v	LCD bias voltage level 1	—	0.34	—	Vvdd_3v	—
Vlcd_vll0_3v	LCD bias voltage level 0	—	0	—	Vvdd_3v	—
Vlcd_error	LCD bias voltage error	-50	0	50	mV	—
Vlcd_config_step	LCD bias voltage config step for Vlcd_vll2_3v and Vlcd_vll1_3v	—	1.67%	—	Vvdd_3v	—
tstart	Startup time	—	—	10	ms	—
fframe	LCD frame frequency	28	30	58	Hz	—

6 Package dimensions

6.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
WFBGA169	98ASA02230D
LQFP144	98ASS23177W
LQFP100	98ASS23308W
LQFP64	98ASS23234W

7 Pinout

7.1 MCX A175, A176, A185, A186, A255, A256, A265, and A266 Signal Multiplexing and Pin Assignments

The signal multiplexing and pin assignments are provided in following link:

- MCXA17x_18x_25x_26x_pinout.xlsx

The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

However, the pinout table is as given below

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Table 49. Pinmux

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
P1_8	1	B2	1	2	**ALT0** - P1_8 **ALT1** - FREQME_CLK_IN0 **ALT2** - LPUART1_RXD **ALT3** - LPI2C2_SDA **ALT4** - CT_INP8 **ALT5** - CT0_MAT2 **ALT6** - FLEXIO0_D16 **ALT7** - SmartDMA_PIO4 **ALT9** - LCD_P6 **ALT10** - I3C0_SDA	**IO Supply** - VDD **Pad type** - HD+I3C **Default** - DIS	**ANALOG** - LCD_P6 **VDD SYS** - WUU0_IN10
P1_9	2	B1	2	3	**ALT0** - P1_9 **ALT1** - FREQME_CLK_IN1 **ALT2** - LPUART1_TXD **ALT3** - LPI2C2_SCL **ALT4** - CT_INP9 **ALT5** - CT0_MAT3 **ALT6** - FLEXIO0_D17 **ALT7** - SmartDMA_PIO5 **ALT9** - LCD_P7 **ALT10** - I3C0_SCL	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	**ANALOG** - LCD_P7
P1_10	3	C2	3	4	**ALT0** - P1_10 **ALT2** - LPUART1_RTS_B **ALT3** - LPI2C2_SDAS **ALT4** - CT2_MAT0 **ALT6** - FLEXIO0_D18 **ALT7** - SmartDMA_PIO6 **ALT8** - LPUART5_TXD **ALT9** - LCD_P8 **ALT11** - CAN0_TXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A8/LCD_P8
P1_11	4	C1	4	5	**ALT0** - P1_11 **ALT1** - TRIG_OUT2 **ALT2** - LPUART1_CTS_B **ALT3** - LPI2C2_SCLS **ALT4** - CT2_MAT1 **ALT6** - FLEXIO0_D19	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A9/LCD_P9 **VDD SYS** - WUU0_IN11

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT7 - SmartDMA_PIO7 **ALT8** - LPUART5_RXD **ALT9** - LCD_P9 **ALT10** - I3C0_PUR **ALT11** - CAN0_RXD		
P1_12	5	D4	5	6	**ALT0** - P1_12 **ALT2** - LPI2C1_SDA **ALT3** - LPUART2_RXD **ALT4** - CT2_MAT2 **ALT6** - FLEXIO0_D20 **ALT7** - SmartDMA_PIO8 **ALT8** - LPUART5_CTS_B **ALT9** - LCD_P10 **ALT11** - CAN1_RXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A10/LCD_P10 **VDD SYS** - WUU0_IN12
P1_13	6	D1	6	7	**ALT0** - P1_13 **ALT1** - TRIG_IN3 **ALT2** - LPI2C1_SCL **ALT3** - LPUART2_TXD **ALT4** - CT2_MAT3 **ALT6** - FLEXIO0_D21 **ALT7** - SmartDMA_PIO9 **ALT8** - LPUART5_RTS_B **ALT9** - LCD_P11 **ALT11** - CAN1_TXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A11/LCD_P11
P1_14	7	E2	7	--	**ALT0** - P1_14 **ALT2** - LPI2C1_SCLS **ALT3** - LPUART2_RTS_B **ALT5** - CT3_MAT0 **ALT6** - FLEXIO0_D22 **ALT7** - SmartDMA_PIO10 **ALT9** - LCD_P12	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A12/LCD_P12
P1_15	8	E1	8	--	**ALT0** - P1_15 **ALT2** - LPI2C1_SDAS **ALT3** - LPUART2_CTS_B **ALT5** - CT3_MAT1	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A13/LCD_P13 **VDD SYS** - WUU0_IN13

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT6 - FLEXIO0_D23 **ALT7** - SmartDMA_PIO11 **ALT9** - LCD_P13		
P1_16	9	D2	--	--	**ALT0** - P1_16 **ALT4** - CT_INP12 **ALT6** - FLEXIO0_D24 **ALT7** - SmartDMA_PIO12 **ALT8** - LPUART5_RXD **ALT9** - LCD_P14 **ALT11** - CAN1_RXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A14/LCD_P14 **VDD SYS** - WUU0_IN14
P1_17	10	D3	--	--	**ALT0** - P1_17 **ALT4** - CT_INP13 **ALT6** - FLEXIO0_D25 **ALT7** - SmartDMA_PIO13 **ALT8** - LPUART5_TXD **ALT9** - LCD_P15 **ALT11** - CAN1_TXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A15/LCD_P15
P1_18	11	E4	--	--	**ALT0** - P1_18 **ALT1** - FREQME_CLK_IN0 **ALT4** - CT3_MAT0 **ALT6** - FLEXIO0_D26 **ALT7** - SmartDMA_PIO14 **ALT8** - LPUART5_RTS_B **ALT11** - CAN0_TXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A16
P1_19	12	E3	--	--	**ALT0** - P1_19 **ALT1** - FREQME_CLK_IN1 **ALT4** - CT3_MAT1 **ALT6** - FLEXIO0_D27 **ALT7** - SmartDMA_PIO15 **ALT8** - LPUART5_CTS_B **ALT11** - CAN0_RXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A17 **VDD SYS** - WUU0_IN15
P1_29	13	F2	9	8	**ALT0** - P1_29 **ALT1** - RESET_B **ALT2** - SPC_LPREQ	**IO Supply** - VDD **Pad type** - RST **Default** - ALT1	**VDD SYS** - RESET_B
P1_30	14	F1	10	9	**ALT0** - P1_30	**IO Supply** - VDD	**ANALOG** - XTAL48M

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT1 - TRIG_OUT3 **ALT3** - LPI2C0_SDA **ALT4** - CT_INP16 **ALT6** - FLEXIO0_D30 **ALT10** - I3C0_SDA	**Pad type** - HD+I3C **Default** - DIS	
P1_31	15	G1	11	10	**ALT0** - P1_31 **ALT1** - TRIG_IN4 **ALT3** - LPI2C0_SCL **ALT4** - CT_INP17 **ALT6** - FLEXIO0_D31 **ALT10** - I3C0_SCL	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	**ANALOG** - EXTAL48M
VSS	16	C3	12	11		**IO Supply** - VDD	
VREFL	17	H5	12	11		**IO Supply** - VDD	
VREFH	18	G5	13	12		**IO Supply** - VDD	
VDD_ANA	19	G6	14	12		**IO Supply** - VDD	
VDD	20	E5	15	13		**IO Supply** - VDD	
P4_0	21	H1	--	--	**ALT0** - P4_0 **ALT1** - TRIG_IN5 **ALT5** - PWM0_A3 **ALT6** - FLEXIO0_D8 **ALT7** - SmartDMA_PIO20	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	
P4_1	22	H2	--	--	**ALT0** - P4_1 **ALT5** - PWM0_B3 **ALT6** - FLEXIO0_D9 **ALT7** - SmartDMA_PIO21	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	
P4_2	23	J1	16	--	**ALT0** - P4_2 **ALT1** - CLKOUT **ALT2** - LPI2C2_SDAS **ALT3** - LPUART3_RXD **ALT4** - CT4_MAT0 **ALT5** - PWM0_A2 **ALT6** - FLEXIO0_D10 **ALT7** - SmartDMA_PIO22	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**VDD SYS** - WUU0_IN16

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
P4_3	24	J2	17	--	**ALT0** - P4_3 **ALT2** - LPI2C2_SCL **ALT3** - LPUART4_TXD **ALT4** - CT4_MAT1 **ALT5** - PWM0_B2 **ALT6** - FLEXIO0_D11 **ALT7** - SmartDMA_PIO23	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	
P4_4	25	K1	18	--	**ALT0** - P4_4 **ALT2** - LPI2C2_SDA **ALT3** - LPUART4_RXD **ALT4** - CT4_MAT2 **ALT5** - PWM0_A1 **ALT6** - FLEXIO0_D12 **ALT7** - SmartDMA_PIO24	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**VDD SYS** - WUU0_IN17
P4_5	26	K2	19	--	**ALT0** - P4_5 **ALT1** - TRIG_OUT3 **ALT2** - LPI2C2_SCLS **ALT3** - LPUART3_TXD **ALT4** - CT4_MAT3 **ALT5** - PWM0_B1 **ALT6** - FLEXIO0_D13 **ALT7** - SmartDMA_PIO25	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	
P4_6	27	L1	20	--	**ALT0** - P4_6 **ALT1** - TRIG_IN4 **ALT2** - LPI2C2_HREQ **ALT3** - LPUART3_CTS_B **ALT4** - CT_INP6 **ALT5** - PWM0_A0 **ALT6** - FLEXIO0_D14 **ALT7** - SmartDMA_PIO26	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	
P4_7	28	L2	21	--	**ALT0** - P4_7 **ALT1** - TRIG_IN5 **ALT3** - LPUART3_RTS_B **ALT4** - CT_INP7 **ALT5** - PWM0_B0	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT6 - FLEXIO0_D15 **ALT7** - SmartDMA_PIO27		
NC	29	--	--	--			
NC	30	--	--	--			
NC	31	--	--	--			
NC	32	--	--	--			
P2_0	33	M1	22	14	**ALT0** - P2_0 **ALT1** - TRIG_IN6 **ALT2** - LPUART0_RXD **ALT3** - LPUART4_CTS_B **ALT4** - CT_INP16 **ALT5** - CT2_MAT0 **ALT6** - FLEXIO0_D8 **ALT7** - SmartDMA_PIO24 **ALT11** - CAN1_RXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A0 **VDD SYS** - WUU0_IN18
P2_1	34	N1	23	15	**ALT0** - P2_1 **ALT1** - TRIG_IN7 **ALT2** - LPUART0_TXD **ALT3** - LPUART4_RTS_B **ALT4** - CT_INP17 **ALT5** - CT2_MAT1 **ALT6** - FLEXIO0_D9 **ALT7** - SmartDMA_PIO25 **ALT11** - CAN1_TXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A0
P2_2	35	M2	24	16	**ALT0** - P2_2 **ALT1** - TRIG_IN6 **ALT2** - LPUART0_RTS_B **ALT3** - LPUART2_TXD **ALT4** - CT_INP12 **ALT5** - CT2_MAT2 **ALT6** - FLEXIO0_D10 **ALT7** - SmartDMA_PIO26	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ISP** - UART_TXD **ANALOG** - ADC0_A4/CMP0_IN0/ DAC0_OUT/CMP1_INN4
P2_3	36	N2	25	17	**ALT0** - P2_3 **ALT1** - TRIG_IN7	**IO Supply** - VDD **Pad type** - SLOW	**ISP** - UART_RXD

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT2 - LPUART0_CTS_B **ALT3** - LPUART2_RXD **ALT4** - CT_INP13 **ALT5** - CT2_MAT3 **ALT6** - FLEXIO0_D11 **ALT7** - SmartDMA_PIO27	**Default** - DIS	**ANALOG** - ADC0_A3/ CMP1_IN0/ADC1_A4 **VDD SYS** - WUU0_IN19
P2_4	37	M3	26	18	**ALT0** - P2_4 **ALT3** - LPUART2_CTS_B **ALT4** - CT_INP14 **ALT5** - CT1_MAT0 **ALT6** - FLEXIO0_D12 **ALT7** - SmartDMA_PIO28	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A1
P2_5	38	N3	27	19	**ALT0** - P2_5 **ALT3** - LPUART2_RTS_B **ALT4** - CT_INP15 **ALT5** - CT1_MAT1 **ALT6** - FLEXIO0_D13 **ALT7** - SmartDMA_PIO29	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A1
P2_6	39	M4	28	20	**ALT0** - P2_6 **ALT1** - TRIG_OUT4 **ALT2** - LPSPI1_PCS1 **ALT3** - LPUART4_RXD **ALT4** - CT_INP18 **ALT5** - CT1_MAT2 **ALT6** - FLEXIO0_D14 **ALT7** - SmartDMA_PIO30	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A3
P2_7	40	N4	29	21	**ALT0** - P2_7 **ALT1** - TRIG_IN5 **ALT3** - LPUART4_TXD **ALT4** - CT_INP19 **ALT5** - CT1_MAT3 **ALT6** - FLEXIO0_D15 **ALT7** - SmartDMA_PIO31	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - VREFI/ ADC1_A7/ADC0_A7
P2_8	41	L4	--	--	**ALT0** - P2_8 **ALT1** - TRIG_OUT3	**IO Supply** - VDD **Pad type** - SLOW	

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT4 - CT3_MAT0 **ALT6** - FLEXIO0_D16	**Default** - DIS	
P2_9	42	K5	--	--	**ALT0** - P2_9 **ALT1** - TRIG_IN4 **ALT4** - CT3_MAT1 **ALT6** - FLEXIO0_D17	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P2_10	43	L5	30	--	**ALT0** - P2_10 **ALT1** - TRIG_OUT5 **ALT3** - LPUART2_TXD **ALT4** - CT3_MAT2 **ALT6** - FLEXIO0_D18 **ALT7** - SmartDMA_PIO14	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P2_11	44	K6	31	--	**ALT0** - P2_11 **ALT1** - TRIG_IN4 **ALT3** - LPUART2_RXD **ALT4** - CT3_MAT3 **ALT6** - FLEXIO0_D19 **ALT7** - SmartDMA_PIO15	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
VSS	45	C11	32	--		**IO Supply** - VDD	
VDD	46	E6	33	--		**IO Supply** - VDD	
P2_12	47	M5	34	22	**ALT0** - P2_12 **ALT1** - USB0_VBUS_DET **ALT2** - LPSPI1_SCK **ALT3** - LPUART1_RXD **ALT4** - CT4_MAT0 **ALT5** - CT0_MAT0 **ALT6** - FLEXIO0_D20 **ALT7** - SmartDMA_PIO16 **ALT11** - CAN0_RXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A5/OPAMP0_INP **VDD SYS** - WUU0_IN20
P2_13	48	N5	35	23	**ALT0** - P2_13 **ALT1** - TRIG_IN8 **ALT2** - LPSPI1_SDO **ALT3** - LPUART1_TXD **ALT4** - CT4_MAT1	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A5/OPAMP0_INN

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT5 - CT0_MAT1 **ALT6** - FLEXIO0_D21 **ALT7** - SmartDMA_PIO17 **ALT11** - CAN0_TXD		
P2_14	49	L6	--	--	**ALT0** - P2_14 **ALT4** - CT4_MAT2 **ALT6** - FLEXIO0_D22	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P2_15	50	M6	36	24	**ALT0** - P2_15 **ALT1** - TRIG_OUT4 **ALT2** - LPSPI1_SDI **ALT3** - LPUART1_RTS_B **ALT4** - CT4_MAT3 **ALT5** - CT0_MAT2 **ALT6** - FLEXIO0_D23 **ALT7** - SmartDMA_PIO18 **ALT11** - CAN1_RXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - OPAMP0_OUT/ADC0_A2/CMP0_INP4 **VDD SYS** - WUU0_IN21
P2_16	51	N6	37	--	**ALT0** - P2_16 **ALT2** - LPSPI1_SDI **ALT3** - LPUART1_RTS_B **ALT4** - CT3_MAT0 **ALT5** - CT0_MAT2 **ALT6** - FLEXIO0_D24 **ALT7** - SmartDMA_PIO19 **ALT11** - CAN1_TXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A6
P2_17	52	N7	38	--	**ALT0** - P2_17 **ALT1** - TRIG_IN9 **ALT2** - LPSPI1_PCS0 **ALT3** - LPUART1_CTS_B **ALT4** - CT3_MAT1 **ALT5** - CT0_MAT3 **ALT6** - FLEXIO0_D25 **ALT7** - SmartDMA_PIO20	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A6
P2_18	53	K8	--	--	**ALT0** - P2_18 **ALT4** - CT3_MAT2 **ALT6** - FLEXIO0_D26	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
P2_19	54	M7	39	--	**ALT0** - P2_19 **ALT1** - TRIG_OUT5 **ALT4** - CT3_MAT3 **ALT6** - FLEXIO0_D27 **ALT7** - SmartDMA_PIO21	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A2/CMP1_INP4
P2_20	55	N8	40	--	**ALT0** - P2_20 **ALT1** - TRIG_IN8 **ALT2** - LPSPI1_PCS2 **ALT4** - CT2_MAT0 **ALT6** - FLEXIO0_D28 **ALT7** - SmartDMA_PIO22	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P2_21	56	M8	41	--	**ALT0** - P2_21 **ALT1** - TRIG_IN9 **ALT2** - LPSPI1_PCS3 **ALT4** - CT2_MAT1 **ALT6** - FLEXIO0_D29 **ALT7** - SmartDMA_PIO23	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P2_22	57	L8	--	--	**ALT0** - P2_22 **ALT4** - CT2_MAT2 **ALT6** - FLEXIO0_D30	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P2_23	58	N9	42	--	**ALT0** - P2_23 **ALT1** - TRIG_OUT5 **ALT4** - CT2_MAT3 **ALT6** - FLEXIO0_D31	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - CMP0_INN4
P2_24	59	M9	--	--	**ALT0** - P2_24 **ALT1** - TRIG_OUT6 **ALT4** - CT_INP8	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P2_25	60	K9	--	--	**ALT0** - P2_25 **ALT1** - TRIG_OUT7 **ALT4** - CT_INP9	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P2_26	61	L9	--	--	**ALT0** - P2_26 **ALT1** - TRIG_IN5 **ALT4** - CT_INP10	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
NC	62	--	--	--			

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
VSS	63	L3	--	--		**IO Supply** - VDD	
VDD	64	E8	--	--		**IO Supply** - VDD	
VDD_USB	65	N11	43	25		**IO Supply** - VDD_USB	
USB0_DM	66	N10	44	26		**IO Supply** - VDD_USB **Pad type** - ANA	**ANALOG** - USB0_DM **VDD SYS** - WUU0_IN28
USB0_DP	67	M10	45	27		**IO Supply** - VDD_USB **Pad type** - ANA	**ANALOG** - USB0_DP **VDD SYS** - WUU0_IN29
VSS	68	L11	46	28		**IO Supply** - VDD	
VDD	69	E9	47	29		**IO Supply** - VDD	
P3_31	70	M12	48	30	**ALT0** - P3_31 **ALT1** - TRIG_IN10 **ALT2** - LPI2C3_SDAS **ALT3** - LPUART4_CTS_B **ALT4** - CT0_MAT3 **ALT6** - FLEXIO0_D31 **ALT7** - PWM1_B0 **ALT10** - SmartDMA_PIO31	**IO Supply** - VDD **Pad type** - SLOW+TAM **Default** - DIS	**ANALOG** - ADC1_A20 **VDD SYS** - LPTMR0_ALT2/TAMPER0
P3_30	71	N12	49	31	**ALT0** - P3_30 **ALT1** - TRIG_OUT6 **ALT2** - LPI2C3_SCLS **ALT3** - LPUART4_RTS_B **ALT4** - CT0_MAT2 **ALT6** - FLEXIO0_D30 **ALT7** - PWM1_A0 **ALT10** - SmartDMA_PIO30	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A21
P3_29	72	N13	50	32	**ALT0** - P3_29 **ALT1** - ISPMODE_N **ALT2** - LPI2C3_HREQ **ALT4** - CT_INP3 **ALT5** - CT3_MAT3 **ALT6** - FLEXIO0_D29 **ALT10** - SmartDMA_PIO29	**IO Supply** - VDD **Pad type** - SLOW+TAM **Default** - DIS	**ANALOG** - ADC1_A22 **VDD SYS** - WUU0_IN27/TAMPER1
P3_28	73	M13	51	33	**ALT0** - P3_28	**IO Supply** - VDD **Pad type** - 5VTOL	**VDD SYS** - WUU0_IN26

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT1 - TRIG_IN11 **ALT2** - LPI2C3_SDA **ALT3** - LPUART4_RXD **ALT4** - CT_INP12 **ALT5** - CT3_MAT2 **ALT6** - FLEXIO0_D28 **ALT7** - PWM1_B3 **ALT10** - SmartDMA_PIO28	**Default** - DIS	
P3_27	74	L12	52	34	**ALT0** - P3_27 **ALT1** - TRIG_OUT7 **ALT2** - LPI2C3_SCL **ALT3** - LPUART4_TXD **ALT4** - CT_INP13 **ALT5** - CT3_MAT1 **ALT6** - FLEXIO0_D27 **ALT7** - PWM1_A3 **ALT10** - SmartDMA_PIO27	**IO Supply** - VDD **Pad type** - 5VTOL **Default** - DIS	**VDD SYS** - WUU0_IN30
P3_26	75	L13	--	--	**ALT0** - P3_26 **ALT1** - TRIG_IN10 **ALT4** - CT_INP14 **ALT6** - FLEXIO0_D26 **ALT10** - SmartDMA_PIO26	**IO Supply** - VDD **Pad type** - SLOW+TAM **Default** - DIS	**VDD SYS** - TAMPER2
P3_25	76	K12	--	--	**ALT0** - P3_25 **ALT1** - TRIG_OUT6 **ALT4** - CT_INP15 **ALT6** - FLEXIO0_D25 **ALT10** - SmartDMA_PIO25	**IO Supply** - VDD **Pad type** - SLOW+TAM **Default** - DIS	**VDD SYS** - TAMPER3
P3_24	77	K13	--	--	**ALT0** - P3_24 **ALT1** - TRIG_IN11 **ALT4** - CT_INP16 **ALT6** - FLEXIO0_D24 **ALT10** - SmartDMA_PIO24	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
NC	78	--	--	--			
NC	79	--	--	--			

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
P3_23	80	J12	--	--	**ALT0** - P3_23 **ALT3** - LPUART1_CTS_B **ALT4** - CT_INP11 **ALT6** - FLEXIO0_D31 **ALT7** - PWM1_X3 **ALT10** - SmartDMA_PIO23	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P3_22	81	J13	53	--	**ALT0** - P3_22 **ALT3** - LPUART1_RTS_B **ALT4** - CT_INP10 **ALT6** - FLEXIO0_D30 **ALT7** - PWM1_X2 **ALT10** - SmartDMA_PIO22	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P3_21	82	H12	54	--	**ALT0** - P3_21 **ALT1** - TRIG_OUT1 **ALT2** - LPI2C3_SCL **ALT3** - LPUART1_TXD **ALT4** - CT2_MAT3 **ALT5** - PWM0_X3 **ALT6** - FLEXIO0_D29 **ALT7** - PWM1_B3 **ALT10** - SmartDMA_PIO21	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P3_20	83	H13	55	--	**ALT0** - P3_20 **ALT1** - TRIG_OUT0 **ALT2** - LPI2C3_SDA **ALT3** - LPUART1_RXD **ALT4** - CT2_MAT2 **ALT5** - PWM0_X2 **ALT6** - FLEXIO0_D28 **ALT7** - PWM1_A3 **ALT10** - SmartDMA_PIO20	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
NC	84	--	--	--			
P3_19	85	J11	56	--	**ALT0** - P3_19 **ALT2** - LPUART4_TXD **ALT4** - CT2_MAT1 **ALT5** - PWM0_X1	**IO Supply** - VDD **Pad type** - SLOW+TAM **Default** - DIS	**ANALOG** - LCD_P47 **VDD SYS** - TAMPER4

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT6 - FLEXIO0_D27 **ALT7** - PWM1_X1 **ALT9** - LCD_P47 **ALT10** - SmartDMA_PIO19		
P3_18	86	J10	57	--	**ALT0** - P3_18 **ALT2** - LPUART4_RXD **ALT4** - CT2_MAT0 **ALT5** - PWM0_X0 **ALT6** - FLEXIO0_D26 **ALT7** - PWM1_X0 **ALT9** - LCD_P46 **ALT10** - SmartDMA_PIO18	**IO Supply** - VDD **Pad type** - SLOW+TAM **Default** - DIS	**ANALOG** - LCD_P46 **VDD SYS** - TAMPER5
P3_17	87	H11	58	--	**ALT0** - P3_17 **ALT2** - LPUART4_CTS_B **ALT4** - CT_INP9 **ALT6** - FLEXIO0_D25 **ALT7** - PWM1_B0 **ALT9** - LCD_P45 **ALT10** - SmartDMA_PIO17	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - LCD_P45
P3_16	88	H10	59	--	**ALT0** - P3_16 **ALT2** - LPUART4_RTS_B **ALT4** - CT_INP8 **ALT6** - FLEXIO0_D24 **ALT7** - PWM1_A0 **ALT9** - LCD_P44 **ALT10** - SmartDMA_PIO16	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - LCD_P44
P3_15	89	G13	60	35	**ALT0** - P3_15 **ALT2** - LPUART2_TXD **ALT3** - LPUART3_RTS_B **ALT4** - CT_INP7 **ALT5** - PWM0_X3 **ALT6** - FLEXIO0_D23 **ALT7** - PWM1_B1 **ALT9** - LCD_P43 **ALT10** - SmartDMA_PIO15	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - LCD_P43

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
P3_14	90	F12	61	36	**ALT0** - P3_14 **ALT2** - LPUART2_RXD **ALT3** - LPUART3_CTS_B **ALT4** - CT_INP6 **ALT5** - PWM0_X2 **ALT6** - FLEXIO0_D22 **ALT7** - PWM1_A1 **ALT9** - LCD_P42 **ALT10** - SmartDMA_PIO14	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - LCD_P42 **VDD SYS** - WUU0_IN25
P3_13	91	F13	62	37	**ALT0** - P3_13 **ALT2** - LPUART2_CTS_B **ALT3** - LPUART3_RXD **ALT4** - CT1_MAT3 **ALT5** - PWM0_X1 **ALT6** - FLEXIO0_D21 **ALT7** - PWM1_B2 **ALT9** - LCD_P41 **ALT10** - SmartDMA_PIO13	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - LCD_P41
P3_12	92	E12	63	38	**ALT0** - P3_12 **ALT2** - LPUART2_RTS_B **ALT3** - LPUART3_TXD **ALT4** - CT1_MAT2 **ALT5** - PWM0_X0 **ALT6** - FLEXIO0_D20 **ALT7** - PWM1_A2 **ALT9** - LCD_P40 **ALT10** - SmartDMA_PIO12	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - LCD_P40
VSS	93	C7	64	--		**IO Supply** - VDD	
VDD	94	J5	65	--		**IO Supply** - VDD	
P3_11	95	E13	66	39	**ALT0** - P3_11 **ALT1** - TRIG_IN6 **ALT2** - LPSPI1_PCS0 **ALT3** - LPUART1_CTS_B **ALT4** - CT1_MAT1 **ALT5** - PWM0_B2	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - LCD_P39 **VDD SYS** - WUU0_IN24

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT6 - FLEXIO0_D19 **ALT8** - LPUART5_RXD **ALT9** - LCD_P39 **ALT10** - SmartDMA_PIO11		
P3_10	96	D13	67	40	**ALT0** - P3_10 **ALT1** - TRIG_IN5 **ALT2** - LPSPI1_SCK **ALT3** - LPUART1_RTS_B **ALT4** - CT1_MAT0 **ALT5** - PWM0_A2 **ALT6** - FLEXIO0_D18 **ALT8** - LPUART5_TXD **ALT9** - LCD_P38 **ALT10** - SmartDMA_PIO10	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - LCD_P38
P3_9	97	D12	68	41	**ALT0** - P3_9 **ALT1** - TRIG_IN4 **ALT2** - LPSPI1_SDI **ALT3** - LPUART1_TXD **ALT4** - CT_INP5 **ALT5** - PWM0_B1 **ALT6** - FLEXIO0_D17 **ALT8** - LPUART5_RTS_B **ALT9** - LCD_P37 **ALT10** - SmartDMA_PIO9	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - LCD_P37
P3_8	98	C13	69	42	**ALT0** - P3_8 **ALT1** - TRIG_IN3 **ALT2** - LPSPI1_SDO **ALT3** - LPUART1_RXD **ALT4** - CT_INP4 **ALT5** - PWM0_A1 **ALT6** - FLEXIO0_D16 **ALT8** - LPUART5_CTS_B **ALT9** - LCD_P36 **ALT10** - SmartDMA_PIO8 **ALT12** - CLKOUT	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - LCD_P36 **VDD SYS** - WUU0_IN23

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
P3_7	99	C12	70	43	**ALT0** - P3_7 **ALT1** - TRIG_IN2 **ALT2** - LPSPI1_PCS2 **ALT3** - LPUART3_CTS_B **ALT4** - CT4_MAT3 **ALT5** - PWM0_B3 **ALT6** - FLEXIO0_D15 **ALT7** - PWM1_B0 **ALT9** - LCD_P35 **ALT10** - SmartDMA_PIO7	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - LCD_P35
P3_6	100	B13	71	44	**ALT0** - P3_6 **ALT1** - CLKOUT **ALT2** - LPSPI1_PCS3 **ALT3** - LPUART3_RTS_B **ALT4** - CT4_MAT2 **ALT5** - PWM0_A3 **ALT6** - FLEXIO0_D14 **ALT7** - PWM1_A0 **ALT9** - LCD_P34 **ALT10** - SmartDMA_PIO6 **ALT12** - FREQME_CLK_OUT1	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - LCD_P34
P3_5	101	F11	--	--	**ALT0** - P3_5 **ALT4** - CT_INP19 **ALT5** - PWM0_X3 **ALT6** - FLEXIO0_D13 **ALT10** - SmartDMA_PIO5	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P3_4	102	F10	--	--	**ALT0** - P3_4 **ALT4** - CT_INP18 **ALT5** - PWM0_X2 **ALT6** - FLEXIO0_D12 **ALT10** - SmartDMA_PIO4	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P3_3	103	E11	--	--	**ALT0** - P3_3 **ALT4** - CT4_MAT1 **ALT5** - PWM0_X1	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT6 - FLEXIO0_D11 **ALT7** - PWM1_X3 **ALT10** - SmartDMA_PIO3		
P3_2	104	E10	--	--	**ALT0** - P3_2 **ALT2** - LPSPI1_PCS1 **ALT4** - CT4_MAT0 **ALT5** - PWM0_X0 **ALT6** - FLEXIO0_D10 **ALT7** - PWM1_X2 **ALT10** - SmartDMA_PIO2	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P3_1	105	B12	72	45	**ALT0** - P3_1 **ALT1** - TRIG_IN1 **ALT3** - LPUART3_TXD **ALT4** - CT_INP17 **ALT5** - PWM0_B0 **ALT6** - FLEXIO0_D9 **ALT7** - PWM1_X1 **ALT9** - LCD_P33 **ALT10** - SmartDMA_PIO1 **ALT12** - FREQME_CLK_OUT0	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	**ANALOG** - LCD_P33
P3_0	106	A13	73	46	**ALT0** - P3_0 **ALT1** - TRIG_IN0 **ALT3** - LPUART3_RXD **ALT4** - CT_INP16 **ALT5** - PWM0_A0 **ALT6** - FLEXIO0_D8 **ALT7** - PWM1_X0 **ALT9** - LCD_P32 **ALT10** - SmartDMA_PIO0	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	**ANALOG** - LCD_P32 **VDD SYS** - WUU0_IN22
VSS	107	D7	74	47		**IO Supply** - VDD	
VDD	108	J6	75	48		**IO Supply** - VDD	
P0_0	109	A12	76	49	**ALT0** - P0_0 **ALT1** - TMS/SWDIO **ALT2** - LPUART0_RTS_B	**IO Supply** - VDD **Pad type** - SLOW **Default** - ALT1	

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT3 - LPSPI0_PCS0 **ALT4** - CT_INP0 **ALT6** - FLEXIO0_D0		
P0_1	110	B11	77	50	**ALT0** - P0_1 **ALT1** - TCLK/SWCLK **ALT2** - LPUART0_CTS_B **ALT3** - LPSPI0_SDI **ALT4** - CT_INP1 **ALT6** - FLEXIO0_D1	**IO Supply** - VDD **Pad type** - SLOW **Default** - ALT1	
P0_2	111	A11	78	51	**ALT0** - P0_2 **ALT1** - TDO/SWO **ALT2** - LPUART0_RXD **ALT3** - LPSPI0_SCK **ALT4** - CT0_MAT0 **ALT5** - UTICK_CAP0 **ALT6** - FLEXIO0_D2 **ALT10** - I3C0_PUR	**IO Supply** - VDD **Pad type** - SLOW **Default** - ALT1	
P0_3	112	D10	79	52	**ALT0** - P0_3 **ALT1** - TDI **ALT2** - LPUART0_TXD **ALT3** - LPSPI0_SDO **ALT4** - CT0_MAT1 **ALT5** - UTICK_CAP1 **ALT6** - FLEXIO0_D3 **ALT8** - CMP0_OUT	**IO Supply** - VDD **Pad type** - SLOW **Default** - ALT1	**ANALOG** - CMP1_IN1/ADC0_A14
P0_4	113	A10	--	--	**ALT0** - P0_4 **ALT4** - CT0_MAT2 **ALT5** - UTICK_CAP2 **ALT6** - FLEXIO0_D4 **ALT7** - SmartDMA_PIO0 **ALT8** - CMP1_OUT	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**VDD SYS** - WUU0_IN0
P0_5	114	B9	--	--	**ALT0** - P0_5 **ALT4** - CT0_MAT3 **ALT5** - UTICK_CAP3 **ALT6** - FLEXIO0_D5	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT7 - SmartDMA_PIO1		
P0_6	115	A9	80	53	**ALT0** - P0_6 **ALT1** - ISPMODE_N **ALT2** - LPI2C0_HREQ **ALT3** - LPSPI0_PCS1 **ALT4** - CT_INP2 **ALT6** - FLEXIO0_D6 **ALT7** - SmartDMA_PIO2 **ALT8** - CMP1_OUT **ALT12** - CLKOUT	**IO Supply** - VDD **Pad type** - SLOW **Default** - ALT1	**ISP** - ISPMODE_N **ANALOG** - ADC0_A15
P0_7	116	D11	--	--	**ALT0** - P0_7 **ALT4** - CT_INP3 **ALT6** - FLEXIO0_D7 **ALT7** - SmartDMA_PIO3	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**VDD SYS** - WUU0_IN1
NC	117	--	--	--		**IO Supply** - NC	
VSS	118	E7	--	--		**IO Supply** - VDD	
P0_12	119	C10	--	--	**ALT0** - P0_12 **ALT4** - CT0_MAT2 **ALT6** - FLEXIO0_D4 **ALT9** - LCD_P16	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - LCD_P16
P0_13	120	B10	--	--	**ALT0** - P0_13 **ALT4** - CT0_MAT3 **ALT6** - FLEXIO0_D5 **ALT9** - LCD_P17	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - LCD_P17
P0_14	121	C9	81	--	**ALT0** - P0_14 **ALT4** - CT_INP2 **ALT5** - UTICK_CAP0 **ALT6** - FLEXIO0_D6 **ALT7** - SmartDMA_PIO4 **ALT9** - LCD_P18	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - LCD_P18
P0_15	122	D9	82	--	**ALT0** - P0_15 **ALT4** - CT_INP3 **ALT5** - UTICK_CAP1 **ALT6** - FLEXIO0_D7	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - LCD_P19

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT7 - SmartDMA_PIO5 **ALT9** - LCD_P19		
P0_16	123	B8	83	54	**ALT0** - P0_16 **ALT2** - LPI2C0_SDA **ALT3** - LPSPI0_PCS2 **ALT4** - CT0_MAT0 **ALT5** - UTICK_CAP2 **ALT6** - FLEXIO0_D0 **ALT7** - SmartDMA_PIO6 **ALT9** - LCD_P20 **ALT10** - I3C0_SDA	**IO Supply** - VDD **Pad type** - HD+I3C **Default** - DIS	**ANALOG** - LCD_P20 **VDD SYS** - WUU0_IN2
P0_17	124	A8	84	55	**ALT0** - P0_17 **ALT2** - LPI2C0_SCL **ALT3** - LPSPI0_PCS3 **ALT4** - CT0_MAT1 **ALT5** - UTICK_CAP3 **ALT6** - FLEXIO0_D1 **ALT7** - SmartDMA_PIO7 **ALT9** - LCD_P21 **ALT10** - I3C0_SCL	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	**ANALOG** - LCD_P21
P0_18	125	A7	85	--	**ALT0** - P0_18 **ALT2** - LPI2C0_SCLS **ALT4** - CT0_MAT2 **ALT6** - FLEXIO0_D2 **ALT7** - SmartDMA_PIO8 **ALT8** - CMP0_OUT **ALT9** - LCD_P22	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A8/LCD_P22
P0_19	126	B7	86	--	**ALT0** - P0_19 **ALT2** - LPI2C0_SDAS **ALT4** - CT0_MAT3 **ALT6** - FLEXIO0_D3 **ALT7** - SmartDMA_PIO9 **ALT8** - CMP1_OUT **ALT9** - LCD_P23	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A9/LCD_P23 **VDD SYS** - WUU0_IN3

Table continues on the next page...

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
P0_20	127	A6	87	--	**ALT0** - P0_20 **ALT3** - LPUART0_RXD **ALT4** - CT_INP0 **ALT6** - FLEXIO0_D4 **ALT7** - SmartDMA_PIO10 **ALT9** - LCD_P24	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A10/LCD_P24 **VDD SYS** - WUU0_IN4
P0_21	128	B6	88	--	**ALT0** - P0_21 **ALT3** - LPUART0_TXD **ALT4** - CT_INP1 **ALT6** - FLEXIO0_D5 **ALT7** - SmartDMA_PIO11 **ALT9** - LCD_P25	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A11/LCD_P25
P0_22	129	C8	89	--	**ALT0** - P0_22 **ALT3** - LPUART0_RTS_B **ALT4** - CT_INP2 **ALT5** - CT0_MAT0 **ALT6** - FLEXIO0_D6 **ALT7** - SmartDMA_PIO12 **ALT9** - LCD_P26	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A12/LCD_P26
P0_23	130	D8	90	--	**ALT0** - P0_23 **ALT3** - LPUART0_CTS_B **ALT4** - CT_INP3 **ALT5** - CT0_MAT1 **ALT6** - FLEXIO0_D7 **ALT7** - SmartDMA_PIO13 **ALT9** - LCD_P27	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A13/LCD_P27 **VDD SYS** - WUU0_IN5
P0_24	131	C6	--	--	**ALT0** - P0_24 **ALT4** - CT0_MAT0 **ALT8** - LPUART5_RXD **ALT9** - LCD_P28	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - LCD_P28
P0_25	132	D6	--	--	**ALT0** - P0_25 **ALT4** - CT0_MAT1 **ALT8** - LPUART5_TXD **ALT9** - LCD_P29	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - LCD_P29
P0_26	133	C5	--	--	**ALT0** - P0_26	**IO Supply** - VDD	**ANALOG** - LCD_P30

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
					ALT4 - CT0_MAT2 **ALT8** - LPUART5_RTS_B **ALT9** - LCD_P30	**Pad type** - SLOW **Default** - DIS	
P0_27	134	D5	--	--	**ALT0** - P0_27 **ALT4** - CT0_MAT3 **ALT8** - LPUART5_CTS_B **ALT9** - LCD_P31	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - LCD_P31
P1_0	135	A5	91	56	**ALT0** - P1_0 **ALT1** - TRIG_IN0 **ALT2** - LPSPI0_SDO **ALT3** - LPI2C1_SDA **ALT4** - CT_INP4 **ALT5** - CT0_MAT2 **ALT6** - FLEXIO0_D8 **ALT9** - LCD_P0 **ALT11** - CAN1_RXD	**IO Supply** - VDD **Pad type** - MED+I2C_FILT **Default** - DIS	**ANALOG** - ADC0_A16/CMP0_IN3/LCD_P0 **VDD SYS** - WUU0_IN6/LPTMR0_ALT3
P1_1	136	B5	92	57	**ALT0** - P1_1 **ALT1** - TRIG_IN1 **ALT2** - LPSPI0_SCK **ALT3** - LPI2C1_SCL **ALT4** - CT_INP5 **ALT5** - CT0_MAT3 **ALT6** - FLEXIO0_D9 **ALT9** - LCD_P1 **ALT11** - CAN1_TXD	**IO Supply** - VDD **Pad type** - MED+I2C_FILT **Default** - DIS	**ANALOG** - ADC0_A17/CMP1_IN3/LCD_P1
P1_2	137	A4	93	58	**ALT0** - P1_2 **ALT1** - TRIG_OUT0 **ALT2** - LPSPI0_SDI **ALT3** - LPI2C1_SDAS **ALT4** - CT1_MAT0 **ALT5** - CT_INP0 **ALT6** - FLEXIO0_D10 **ALT9** - LCD_P2 **ALT11** - CAN0_TXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_A18/LCD_P2

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
P1_3	138	B4	94	59	**ALT0** - P1_3 **ALT1** - TRIG_OUT1 **ALT2** - LPSPI0_PCS0 **ALT3** - LPI2C1_SCLS **ALT4** - CT1_MAT1 **ALT5** - CT_INP1 **ALT6** - FLEXIO0_D11 **ALT9** - LCD_P3 **ALT11** - CAN0_RXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_A19/ CMP0_IN1/LCD_P3 **VDD SYS** - WUU0_IN7
VDD	139	J8	95	60		**IO Supply** - VDD	
VSS	140	F7	96	61		**IO Supply** - VDD	
P1_4	141	A3	97	62	**ALT0** - P1_4 **ALT1** - FREQME_CLK_IN0 **ALT2** - LPSPI0_PCS3 **ALT3** - LPUART2_RXD **ALT4** - CT1_MAT2 **ALT6** - FLEXIO0_D12 **ALT7** - SmartDMA_PIO0	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_A20/ CMP0_IN2/LCD_VLL2 **VDD SYS** - WUU0_IN8
P1_5	142	B3	98	63	**ALT0** - P1_5 **ALT1** - FREQME_CLK_IN1 **ALT2** - LPSPI0_PCS2 **ALT3** - LPUART2_TXD **ALT4** - CT1_MAT3 **ALT6** - FLEXIO0_D13 **ALT7** - SmartDMA_PIO1	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_A21/ CMP1_IN2/LCD_VLL1
P1_6	143	A2	99	64	**ALT0** - P1_6 **ALT1** - TRIG_IN2 **ALT2** - LPSPI0_PCS1 **ALT3** - LPUART2_RTS_B **ALT4** - CT_INP6 **ALT5** - CT4_MAT0 **ALT6** - FLEXIO0_D14 **ALT7** - SmartDMA_PIO2 **ALT9** - LCD_P4 **ALT11** - CAN1_TXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_A22/LCD_P4

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Table 49. Pinmux...*continued*

Pin Name	MCXA26xA25xA18xA17x LQFP144	MCXA26xA25xA18xA17x WFBGA169	MCXA26xA25xA18xA17x LQFP100	MCXA26xA25xA18xA17x LQFP64	Pinmux Assignment	Pad Settings	Alternate Functions
P1_7	144	A1	100	1	**ALT0** - P1_7 **ALT1** - TRIG_OUT2 **ALT3** - LPUART2_CTS_B **ALT4** - CT_INP7 **ALT5** - CT4_MAT1 **ALT6** - FLEXIO0_D15 **ALT7** - SmartDMA_PIO3 **ALT9** - LCD_P5 **ALT11** - CAN1_RXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_A23/LCD_P5 **VDD SYS** - WUU0_IN9
VSS	--	G7,H7,J7,K7,L7,G2,G3,G4,G10,G11,G12,F5,F6,F8,F9,H6,H8,H9,M11	--	--			
VDD	--	J9	--	--			
NC	--	C4, F3, F4, G8, G9, H3, H4, J3, J4, K3, K4, K10, K11, L10	--	--			

Note:

- +I3C in Pad Type represents that strong pull up resistor is implemented on the pin. PV bit is implemented in Pin Control register of the pin.
- 2. +I2C_FILT in Pad Type represents that I2C filter is implemented on the pin. PFE bit is implemented in Pin Control register of the pin.
- 3. HD in Pad Type represents that the pin can support up to 20mA drive strength. I2C filter is implemented on the pin. PFE bit is implemented in Pin Control register of the pin.
- 5VTOL in Pad Type represents that the pin is 5V tolerant.
- DIS in default column represents that the pin's input buffer is disabled by default
- RST pads support passive filter and 1M Ω pull resistor. PFE and PV bits are implemented in Pin Control register of the pin.
- PE, PS, SRE, ODE and DSE are supported in Pin Control register of all types of IO.
- 5VTol and HD pads support two DSE bits in Pin Control register of the pin.
- SLOW in Pad Type represents the IO supports 25MHz. MED in Pad Type represents the IO supports 50MHz.
- +TAM in Pad Type represents the IO supports 1M Ω pull resistor.
- CAN1, LPUART5, SLCD are not available in MCXA17x and MCXA25x.
- P0_6 is the ISP_ENTRY pin to for WFBGA169, LQFP144, LQFP100, and LQFP64 package. P3_29 is the ISP_ENTRY pin for QFN32 package.

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7.2 MCX A175, A176, A185, A186, A255, A256, A265, and A266 Pinouts

The pinouts are provided in following link:

- MCXA17x_18x_25x_26x_pinout.xlsx

7.3 Recommended connection for unused analog and digital pins

Table 50 shows the recommended connections for pins if those pins are not used in the customer's application

Table 50. Recommended connection for unused analog and digital pins

Pin Type	Pin Function	Recommendation	Comments
Power	VDD	Must be powered	VDD is the IO supply of P0,P1,P2 and P4, and supplies internal modules including Flash, CMP, and etc.. It must be on
Power	VDD_ANA	Must be powered	VDD_ANA must be same level with VDD, and ramps up together with VDD
Power	VDD_USB	Tie to ground through a 10 kΩ resistor if VDD_USB is an independent pin in the package version used	
Power	VREFH	Always connect to VDD_ANA potential	Always connect to VDD_ANA potential
Power	VREFL	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_ANA	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_USB	Always connect to VSS potential	Always connect to VSS potential
Analog/non-GPIO	ADC*n_x*	Float	
Analog/non-GPIO	ADC*n_x*/DAC*n*_OUT	Float	
Analog/non-GPIO	EXTAL	Float	
Analog/non-GPIO	XTAL	Float	Analog output - Float
Analog/non-GPIO	USB0_DP	Float	Float
Analog/non-GPIO	USB0_DM	Float	Float
GPIO/Analog	Px/ADC*n_x*	Float	Float (default is analog input)
GPIO/Analog	Px/CMP*n*_IN*x*	Float	Float (default is analog input)
GPIO/Digital	JTAG_TCLK	Float	Float (default is JTAG with pulldown)
GPIO/Digital	JTAG_TDI	Float	Float (default is JTAG with pullup)
GPIO/Digital	JTAG_TDO	Float	Float (default is JTAG with pullup)
GPIO/Digital	JTAG_TMS	Float	Float (default is JTAG with pullup)
GPIO/Digital	Px	Float	Float (default is disabled)

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8 Ordering parts

8.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to nxp.com and perform a part number search for the following device numbers: MCXA256

9 Part identification

Part numbers for the device have fields that identify the specific part. Use the values of these fields to determine the specific part.

9.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

9.2 Part number format

Part numbers for this device have the following format:

B PS F C D FS T PG SR PT

Table 51. Part number fields descriptions

Field	Description	Values
B	Brand	• MCX
PS	Product series name	• A
F	Family	• 1 = Baseline • 2 = Baseline Enhance
C	Core Features	• 5 = 180 MHz, 2xADC, 2xMotor PWM, 5xUART, 1xCAN, 1xUSB, 1xFlexIO, Security • 6 = 240 MHz, 2xADC, 2xMotor PWM, 6xUART, 2xCAN, 1xUSB, 1xFlexIO, SLCD, Security • 7 = 180 MHz, 2xADC, 2x Motor PWM, 5xUART, 1x CAN, 1xUSB, 1xFlexIO • 8 = 240 MHz, 2xADC, 2x Motor PWM, 6xUART, 2x CAN, 1xUSB, 1xFlexIO, SLCD
FS	Flash Size	• 5 = 512 KB • 6 = 1024 KB
T	Junction Temperature range (°C)	• V = –40 to 125 °C
PG	Package	• LH = LQFP64 • LL = LQFP100 • LQ = LQFP144

Table continues on the next page...

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Table 51. Part number fields descriptions...*continued*

Field	Description	Values
		• PN = WFBGA169
SR	Silicon Revision	• A = Initial Mask set • B = 1st Major spin • C = 2nd Major spin
PT	Package Type	• R = Tape and Reel • T = Tray

9.3 Example

This is an example part number:

MCXA256VLH

9.4 Small package marking

9.4.1 Package marking information

Table 52. Package Marking

Line	LQFP144	LQFP100	LQFP64	WFBGA169
First Line	AAAAAAAAAA	AAAAAAAAAA	AAAAAAA	AAAAAA
Second Line	MMMMM	MMMMM	AAA MMMMM	MMMMM
Third Line	XXXXYYWWXX	XXXXYYWWXX	XXXXYYWWXX	XXXYWXX

Table 53. Package marking

Identifier	Description
A	Part number code, refer to Ordering Information
M	Mask set
Y	Year
W	Work week
X	NXP internal use

10 Terminology and guidelines

10.1 Definitions

Key terms are defined in the following table:

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Table 54. Definitions

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. ***Note:*** *The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.*
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions ***Note:*** *Typical values are provided as design guidelines and are neither tested nor guaranteed.*

10.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

EXAMPLE
EXAMPLE
EXAMPLE

Figure 28. Examples

10.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

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Table 55. Typical-value conditions

Symbol	Description	Value	Unit
TA	Ambient temperature	25	°C
VDD	Supply voltage	3.3	V

Note: *Typical values are based on characterization but not covered by test limits in production.*

10.4 Relationship between ratings and operating requirements

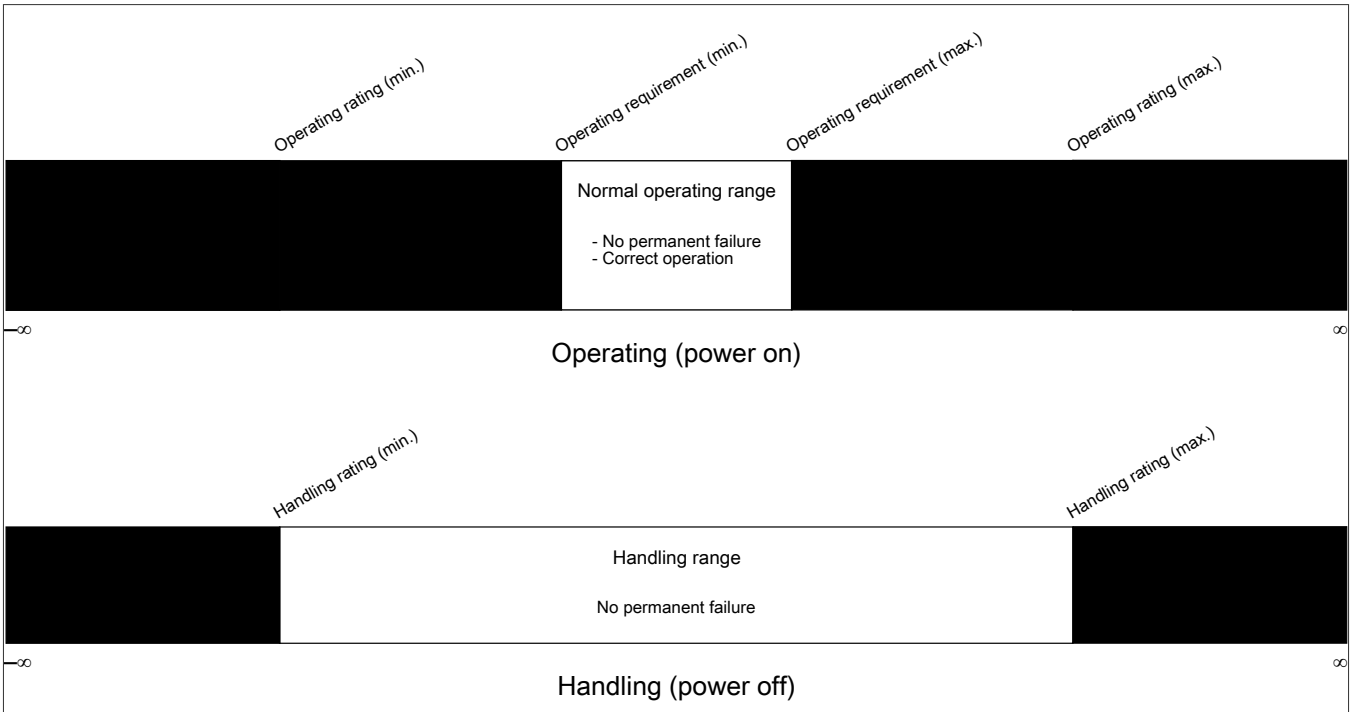


Figure 29. Relationship between ratings and operating requirements

10.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

10.6 Specification Test Methods

Each specification is tested using one of these methods.

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Table 56. Specification test methods

Code	Method	Description
P	Production direct	On every chip during production, testing the specification
I	Production indirect	On every chip during production, testing parts of a module that affect whether the chip meets the specification but not testing the specification itself
C	Characterization on a production tester	Measuring a statistically significant number of sample chips across process (matrix lot), voltage, and temperature ***Note:*** *Typical values are not necessarily characterized across process.*
L	Characterization on lab equipment or a nonproduction tester	
D	Guaranteed by design	Specification based on scientific and engineering principles
O	Other	Using methods such as: • Performing silicon simulations • Performing package thermal simulations • Calculating specifications using reliability data

11 Revision history

The following table provides a revision history for this document.

Table 57. Revision history

Document ID	Release Date	Description
MCXAP144M240F61 v.5	6 July 2026	• Updated the WFBGA part numbers in Table 1 • Added Table 2 • Updated HMI features in Table 5 • Added Table 6 • Removed Section System Crystal Oscillator Specification • Updated Table 24 • Updated the title of Table 25 • Removed TJ, Vvdda, and Vvdd from Table 26 • Added 550 MHz PLL electrical specifications • Updated the description of Tnvmretp10k in Table 32 • Updated the first line of WFBGA169 in Table 52
MCXAP144M240F61 v.4	10 February 2026	• Updated descriptions about FlexPWM in Front matter

Table continues on the next page...

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Table 57. Revision history...*continued*

Document ID	Release Date	Description
		• Added two notes for the Block diagram • Updated the segment LCD in Feature comparison table • Updated the footnote of Table. Voltage and current operating behaviors • Removed Fclkout_1T and updated Δfclkout in Table. FRO180M specifications • Updated ffro16k and Δffro16k in Table. FRO16K specifications • Updated the ALT0 function of P2_1 in Pinout table
MCXAP144M240F61 v.3	14 November 2025	• Updated descriptions of FRO180M, Code Watchdog and CTimer in Section Features • Added MCXA18x and MCXA26x parts in the data sheet • Updated the front matter and feature comparison section • Updated Related resources table and Ordering Information table • Updated the block diagram and bus matrix diagram • Updated Power consumption operating behaviours • Updated Device clock specifications • Added units in JTAG debug interface timing • Updated System Oscillator Crystal Specifications table • Updated Table. FRO180M specifications • Updated INL and DNL parameters of ADC electrical characteristics • Updated second reference of LP9 from slow speed to medium speed in LPSPI controller mode timing • Updated the condition of third instance of LP1 from Peripheral Rx to Peripheral Tx in OD mode in LPSPI peripheral mode timing • Added Segment LCD electrical specifications • Updated the pinout table • Updated Part number fields descriptions table
MCXAP144M240F61 v.2	11 June 2025	• Updated MCXA275 and MCXA276 by MCXA255 and MCXA256 all over the document • Updated the block diagram and bus matrix • Removed the part number list box in front matter • Updated TBDs in front matter • Updated Feature Comparison table • Updated Ordering Information • Removed the Note after block diagram

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Table 57. Revision history*...continued*

Document ID	Release Date	Description
		• Updated Thermal attributes section • Added I/O mux resistance table • Removed CT parameter from 12-bit DAC operating behaviors • Updated FIRC to FRO180M in power mode transition operating behaviours section • Removed INL and DNL parameters for the power supply below 1.71V from Comparator and 8-bit DAC electrical specifications • Added figures of Comparator and 8-bit DAC electrical specifications • Updated I2C HS mode timing electrical specifications • Updated Op-amp to OpAmp and OpAmp electrical specifications • Updated I3C Push-Pull Timing Parameters for SDR mode • Updated the maximum value of Tstart in System oscillator crystal electrical specifications • Added document number of package drawing of WFBGA169 • Updated the Package marking information section • Added space between MCX and A to unify the device name and family in data sheet • Updated master to controller and slave to peripheral in LPSPI module to align with inclusive language • Updated the values in Power mode transition operating behaviours table • Updated the values in Power consumption operating behaviours table • Updated Thermal attributes section • Removed Debug trace operating behaviours table • Updated the values of JTAG Debug Interface Timing • Added S4 and updated the other values in Serial Wire Debug (SWD) Timing specifications • Updated the operator in description of tpgmpg_lifetime for 128 B and tpgmphr_initial for 16 B in Flash command time specifications • Updated TBDs and added K to Nnvmcyc256k in Flash reliability specifications table • Updated the values in LPSPI controller mode timing and LPSPI peripheral mode timing • Added FlexCAN description • Removed Segment LCD electrical specification • Updated the pinout table

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Table 57. Revision history*...continued*

Document ID	Release Date	Description
		• Updated comments in VDD_ANA in Recommended connection for unused analog and digital pins • Removed leakage current for all pins in Voltage and current operating behaviours • Added Note in package diagram in front page "All information on the package WFBGA169 is preliminary and pending qualification"
MCXAP144M240F61 v.1	December 2024	• Initial version

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Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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